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MOBILE COMMUNICATION SYSTEM USING VHDL

Ch Das Prakash
Gitam Rushikonda,
Visakhapatnam, A.P,
India

N Amaralingeswara Rao
BVSR Engg College

ABSTRACT

For the third generation mobile radio communication system (known as 3G), CDMA has become the mainstream air interface. The design is a simplified CDMA communication system, focusing on the most prominent features of a CDMA mobile system-spread spectrum communication. The goal of the project is to design a base station and a user mobile. CDMA air interface design strategies are adopted in protocol (IS-95), frame design as well as data processing design. The communication system designed is capable of multiple user communication with some CDMA characteristics. When compared with GSM mobile communication, CDMA finds better application in effective usage channel band width, speed, are occupancy and even power consumption using spread spectrum techniques. The project is mainly based on direct sequence-CDMA techniques. The VHDL code can be simulated to verify its functionality. Then gate level design equivalent will be synthesized targeting FPGA Device. The real physical design will be laid by place and route method. At least the soft-core design is down loaded into chip.

I. INTRODUCTION

Code Division Multiple Access

Code Division Multiple Access (CDMA) is a radically concept in wireless communications. It has gained widespread international acceptance by cellular radio system operators as an upgrade that will dramatically increase both their system capacity and the service quality. CDMA is a form of spread-spectrum, a family of digital communication techniques that have been used in military applications for many years. The core principle of spread spectrum is the use of noise-like carrier waves, and, as the name implies, bandwidths much wider than that required for simple point-to-point communication at the same data rate.

2. CDMA CONCEPTS

In CDMA each user is assigned a unique code sequence (spreading code) it uses to encode its information-bearing signal [1].the receiver, knowing the code sequence of the user, decodes a received signal after the reception and recovers the original data. The spread spreading of the transmitted signal gives to CDMA its multiple access capability. The benefits of the spreading the signals are

- *Multiple access capability*: The receiver can recover a user's data if each user has a unique code from a family that has a low cross-correlation..
- Protection against multi-path interference.
- *Privacy:* The transmitted signal can only be de-spread if the code to the receiver.
- *Interference rejection*: Background noise power is reduced after de-spreading.

2.1 Spread Spectrum:

There are situations when a system may be required to provide secure communication in a hostile environment such that the transmitted signal is not easily detected or recognized by unwanted listeners. This requirement is catered to by a class of signaling techniques collectively known as *spread-spectrum modulation*. The primary advantage of spread-spectrum communication is its ability to reject interference whether it be unintentional interference by another user simultaneously attempting to transmit through the channel, or the intentional interference by a hostile transmitter attempting to jam the transmission. In spread-spectrum signaling the data sequence occupies a bandwidth in excess of the minimum bandwidth necessary to send it. The spectrum spreading is accomplished before transmission through the use of a code that is independent of data sequence. The same code is used in receiver (operating in synchronism with the transmitter) to dispread the received signal so that the original data sequence may be recovered.

2.2 Pseudorandom Number Sequences

Spread spectrum techniques like *direct-sequence spread-spectrum* and *frequency-hop spread-spectrum* techniques rely on the availability of a *pseudo-noise sequence*. A pseudo-noise sequence is a periodic binary sequence with a noise like waveform that is usually generated by means of a *feedback shift register*. The operation is illustrated in Fig... A feedback shift register consists of an ordinary shift register made up of *m* flip-flops and a logic circuit that are interconnected to form a multiloop feedback circuit. The flip-flops in the shift register are regulated by a single timing clock. At each clock pulse, the state of each flip-flop is shifted to the next one down the line. With each clock pulse the logic circuit computes a Boolean function of the states of the flip-flops. The result is then fed back as input to the first flip-flop, thereby preventing the shift register from emptying. The PN sequence so generated is determined by the length *m* of the shift register, its initial state, and the feedback logic.

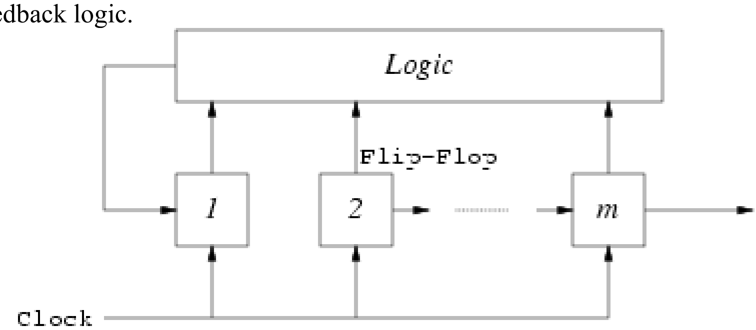


Figure 2.1: Feedback Shift Register

2.3 Classification of Spread Spectrum Techniques

By concept: By concept basis spread spectrum may be considered to be either averaging systems or avoidance systems. An averaging system is one in which the reduction of interference takes place because the interference can be averaged over large time interval. An avoidance system on the other hand is the one in which the reduction of interference occurs because the signal is made to avoid the interference, a large fraction of time.

By Modulation: The most common modulation techniques employed are Directsequence Frequency-Hopping and Time –Hopping

2.4.1 Direct Sequence

In DS-CDMA the modulation information bearing signal is directly modulated by a digital, direct time, discrete value code signal. The data signal can be either analog or digital . In most cases it is digital. In case of digital signal the data modulation is often omitted and the data signal is directly multiplied by the code signal and the resulting signal modulates the wideband carrier. It is from this multiplication that the direct sequence CDMA gets its name.

2.4.2 Frequency –Hopping

In a frequency hopping signal, the frequency is constant in each time chip, but changes from chip to chip. It is frequently convenient to categorized frequency hopping systems as either fast hop or slow hop, since there is a considerable difference in performance for these two types of systems. A fast hop system usually considered to be one in which the frequency hopping takes place at a rate that is greater than the message bit rate. There is of course, an intermediate situation in which the hop rate in the message bit rate are of same order of magnitude.

3. CDMA TRANSMITTER AND RECEIVER

3.1 Direct-Sequence Spread Spectrum with Coherent Binary Phase-Shift Keying

The technique illustrated above was in the context of baseband transmission. To provide for the use of this technique in passband transmission over a satellite channel, for example, *coherent binary phase-shift keying* (BPSK) may be incorporated into the transmitter and receiver as shown in Fig..

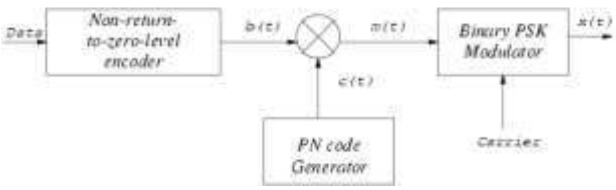


Figure 3.1: DS-CDMA over BFSK Transmitter

The transmitted signal x(t) is thus a direct-sequence binary parse-shift keyed (DS/BPSK) signal. The phase modulation θ(t) of x(t) has one of the two values, 0 and π, depending on the polarities of the message signal b(t) and the PN signal c(t) at time t.

The receiver consists of two stages of demodulation. In the first stage, the received signal and a locally generated carrier are fed to a product modulator. The output of this stage along with a locally generated PN sequence (which is assumed to be synchronized with the PN sequence of the transmitter). The output of this stage is fed to an integrator, which integrates over one bit interval, and finally a decision is made based on the result of integration. A block diagram is shown in Fig..

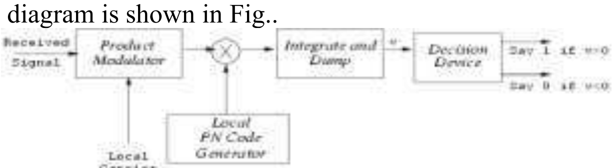


Figure 3.2: DS-CDMA over BFSK Receiver

3.2 Synchronization

Quadrature Phase Shift Keying

Quadrature phase shift keying (QPSK) is a bandwidth conserving scheme, where two consecutive bits are simultaneously transmitted. Like BPSK, the information here is contained in the phase of the transmitted signal. In particular, the phase of the carrier takes on one of the four equally spaced values, π/4,3π/4,5π/4 and 7π/4. Each possible value corresponds to a unique pair of bits called *digit*. A DS/CDMA scheme with QPSK modulation is illustrated in Fig..

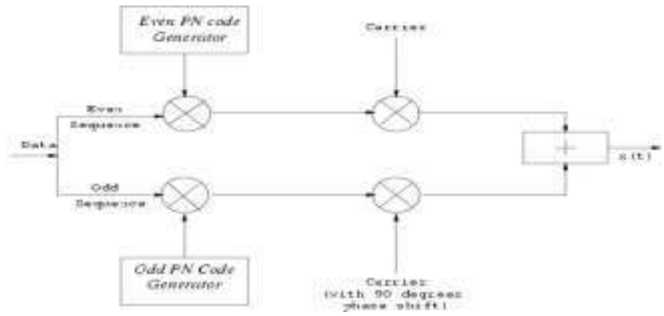


Figure 3.3: DS-CDMA over QFSK Transmitter

3.3 The Transmitter Implementation

3.3.1 Introduction

This chapter describes the implementation of the transmitter used in the project. The transmitter generated a BPSK modulated waveform which was coded to Direct Sequence Code Division Multiple Access (DS-CDMA) waveform and transmitted.

3.3.2 Selection of Frequencies

The TI DSP kit TMS320C5x used has a maximum allowable sampling frequency of 16 kHz. This imposes a maximum frequency limitation of 8 kHz on the transmission frequency. The BPSK frequency and Pseudorandom Number (PN) sequence chip rate were decided to obtain a reasonable waveform within this limit. To obtain a square wave in the 8 kHz limit, a reduced frequency has to be used. Thus the final carrier is limited to 400Hz. As one chip is spread over four carrier cycles the number of chips sent is 100 per second. The length of PN used was 15 chips. This means the bit rate is 100/15 = 6 approximately, bits per second. This bit rate allows sufficient processing time in the DSP chip.

3.3.3 Implementation of the DS coding

The DS sequence used was of length 15 to achieve sufficient spreading. The sequence was precomputed and loaded in the program. The sequence should satisfy the property that shifted versions of it are orthogonal to itself to facilitate synchronization at the receiver. (This hold approximately for the PN sequence of length 15.) Modulating the data with the PN code can be achieved by multiplying the data bit with the PN code. All the 15 chips of the PN code were multiplied within a single bit. This implies a processing gain of 15.

3.3.4 Implementation of the Modulation Scheme

The modulation schemes implemented in the transmitter were Binary Phase shift Keying (BPSK). The block diagram for BPSK receiver was shown in Fig.3.1 For BPSK, each PN coded sequence chip is multiplied with four carrier cycles and transmitted.

Before transmission, the value +1 is converted to 4000h, to increase the positive magnitude and -1 is converted to C000h to increase the negative magnitude.

3.3.5 The Flow Chart for BPSK

The abbreviation AR in the flow chart represents the auxiliary registers used for memory addressing in the DSP chip. The condition checking's have been implemented by keeping counts in the memory. In each iteration, these counts are up dated by bringing the values to accumulator as processing and logical operations are allowed in the accumulator only. Since the carrier used is a square wave, sample values need not be stored in memory but can be directly implemented in multiplication.

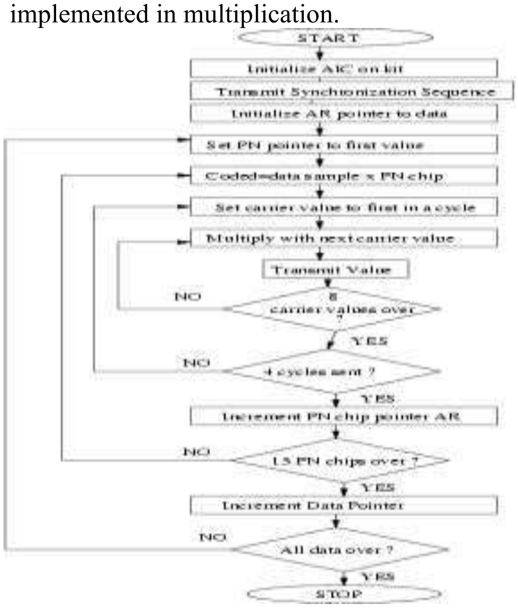


Figure 3.4: Flowchart showing BPSK Transmitter operation

3.4 The Receiver Implementation

Demodulation

The input samples are then threshold to form an ideal square wave. This is necessary as the analog waveform transmitted over the channel suffers from Gibbs phenomenon due to the limited bandwidth of the channel

Data Detection

Each chip is spread over four carrier cycles and there are fifteen chips in one data bit. The multiplication results are summed over the complete fifteen chip period. This produces the value which can be threshold to get the data. If this value is positive, the data was +1, else it was -1. The decoded data is stored at another memory location for viewing. The same is repeated for each data bit. The considerations for condition checking and memory addressing are as in the transmitter.

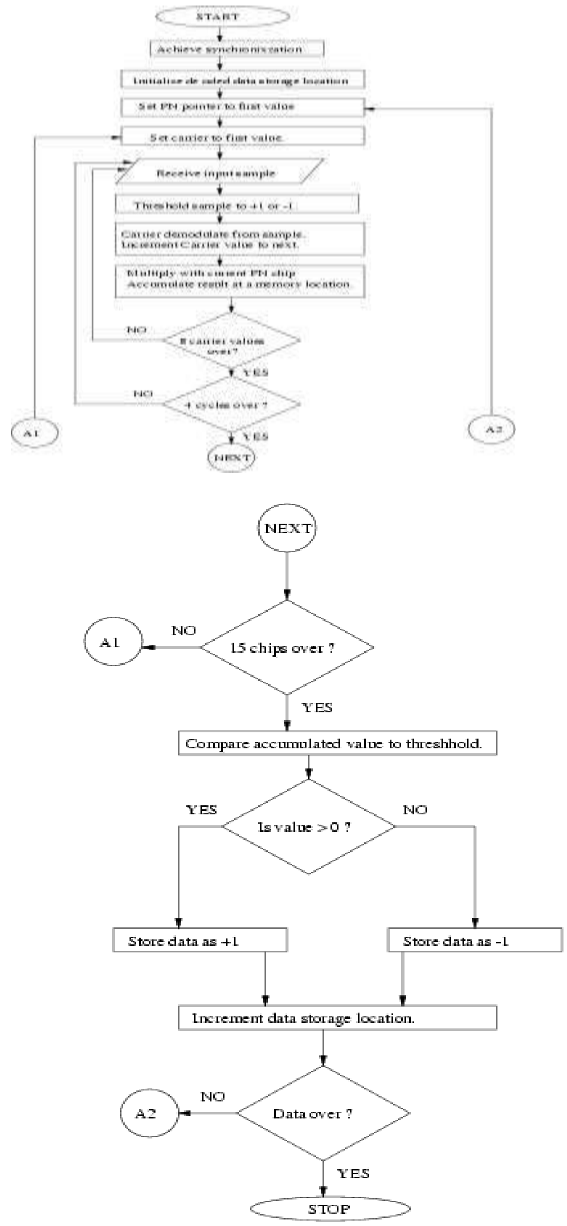
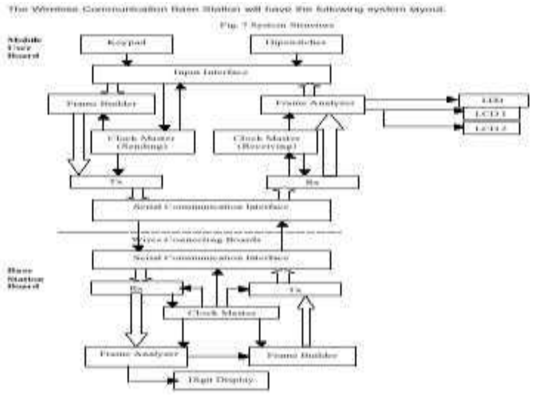


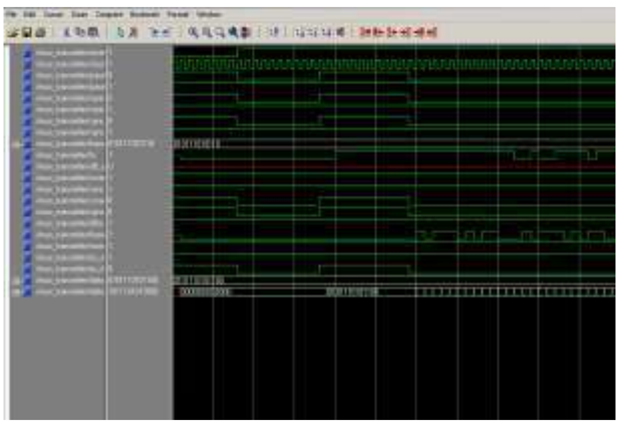
Figure 3.7: The Receiver Flowchart

Layout of wireless communication

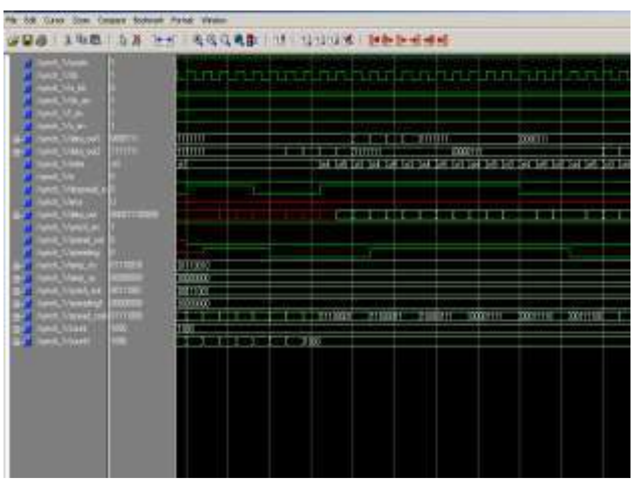


RESULTS

TRANSMITTER OUTPUT



RECEIVER OUTPUT



CONCLUSION

The system is simulated and synthesized at clock frequency provided by the circuit. The maximum possible speed for the mobile user board is 27.39 MHz and for the base station board is 48.78 MHz. Another contribution of the current is that it has system and to accommodate the multiple users.

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