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DESIGN OF 7 STAGE CS-VCO, PHASE DETECTOR AND LOOP FILTER FOR PLL IN 45NM TECHNOLOGY USING CADENCE EDA TOOL

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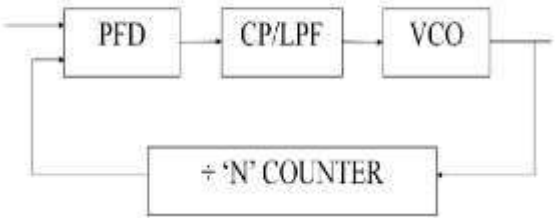
ABSTRACT

Phase Locked Loop is the heart of the many modern electronics as well as communication system. So the PLL must operate in the GHz frequency range. PLL is a mixed signal circuit as its architecture involves both digital and analog signal processing units. This paper focus on design of High-Speed, Low Power Consumption, faster face and frequency locking PLL. All miscellaneous blocks of PLL had been designed in GPDK 45nm CMOS Technology with supply voltage 1.8V using CADENCE spectre tool. Virtuoso Analog Design Environment tool of Cadence have used to design and simulate schematic. Simulation results were done for all process corners, temperature (-40◦C to +100◦c). It is found that designed PLL consumes 865.5 micro-Watts power and have a lock time 100 nanoseconds.

KEYWORDS:*Current limiter, phase detector, transient responses*.

1. INTRODUCTION

The PLL is the most important and developing part of Digital electronics, Communication (Wireless and wire-line) and High-speed (Low propagation delay) digital systems. A PLL designed by Integrated CMOS has achieved the great importance in the last few decades because of the high performance system design in the digital and communication area. It is basically used in clock generator, frequency synthesizer and also used as a data/clock recovery systems in computer, radio-frequency domain and communication system. For designing the PLL wider tuning range, VCO of High gain and high frequency range of operation are required. The PLL consists of PFD (Phase Frequency Detector), Charge pump, Loop filter and VCO (Voltage Control Oscillator) and these three are the basic building blocks of the PLL.



2. BRIEF WORKING

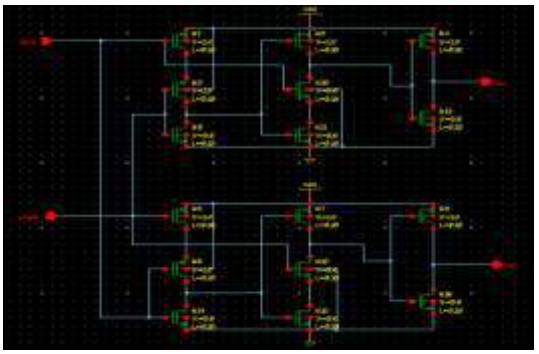
A PFD (Phase Frequency Detector) is used to compare the phase of feedback signal from VCO with the phase of input reference signal and generate outputs (UP or

DOWN) according to the Phase difference. According to the UP or DOWN signal of the PFD, the Charge pump charges or discharges the capacitor of the Low pass filter, and VCO increases or decreases output frequency according to the control voltage produced by the charge pump. The basic block diagram of the PLL is shown.

3. PLL CIRCUIT DESCRIPTION

3.1 Phase Frequency Detector

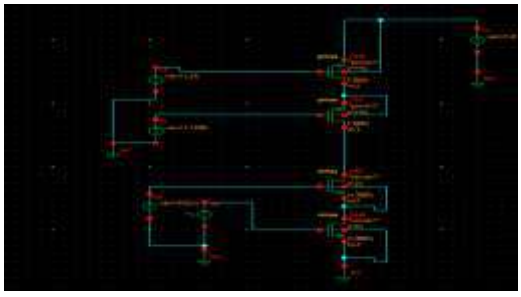
The Phase Frequency Detector (PFD) generates a phase error (UP/DOWN) signal by comparing phase of input (reference) signal and output signal of VCO. UP signal will be HIGH when phase of input (reference) signal leads to VCO output signal otherwise DOWN signal will be HIGH. The below figure shows the Phase Frequency Detector of the proposed PLL designed by the help of four inverters, two pass transistors, two NMOS and two PMOS [1]. Due to the absence of reset circuitry, the proposed PFD is Dead zone free and so that the PFD will produce proper output for any phase difference of input reference signal and output signal of VCO.



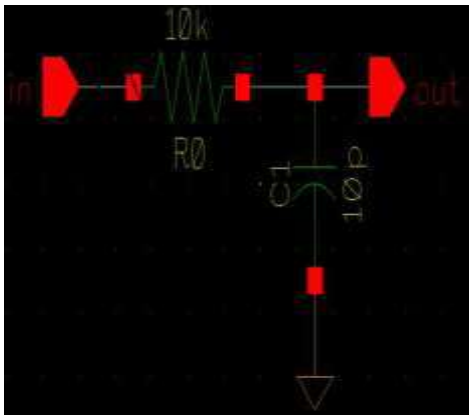
Schematic of Phase Frequency Detector

3.2 Charge Pump and LPF

Charge pump (CP) is used to convert the digital output of PFD into a current signal, so that a stable controllable signal is generated for oscillator to control the oscillation frequency. Charge pump stores the charge in the capacitor of Loop Filter. The below figure shows the schematic of proposed Charge pump (CP) and Low Pass Filter (LPF), operated by the UP and DOWN signals generated by the PFD. When UP signal is HIGH transistor NM1 will be ON and capacitor of LPF starts charging, and when DOWN signal is HIGH transistor NM2 will be ON and capacitor of LPF starts dischargin



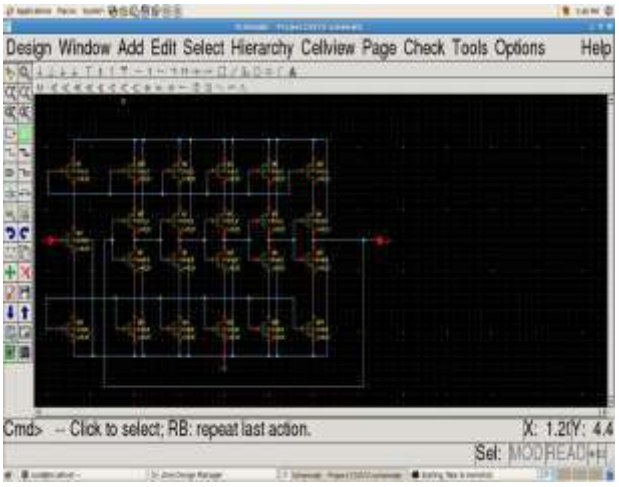
Schematic diagram of Charge Pump



Schematic diagram of LPF

3.3 Proposed VCO for PLL

The VCO plays a vital role in the designing of PLL. Basic function of VCO is to increase or decrease the output frequency according to the input control voltage Figure–4 shows the proposed schematic diagram of CS-VCO (Current Starved Voltage Controlled Oscillator) [3]. In this schematic MP2 and MN2 transistor work as a current limiter for inverter (MP7 and MN7). For five stage CS-VCO, five such inverter with current limiter transistor connected in series. Proposed VCO generates sinusoidal oscillations and last inverter (MP12 and MN12) is used to convert the sinusoidal wave to square wave.



Schematic of Voltage Controlled Oscillator

To determine the design equations for use with the current-starved VCO ,

The total capacitance on the drains of M1 and M2 is given by

Ctot=Cout+Cin

Ctot=Cox*(WpLp+WnLn)+(3/2)*Cox*(WpLp+WnLn)

This is simply the output and input capacitances of the inverter.

The equation can be written as

Ctot=(5/2)*Cox*(WpLp+WnLn) - (*)

The time takes to charge Ctot from zero to Vsp with the constant current Id4 is given by

t1=Ctot*(Vsp/Id4)

While the time takes to discharge Ctot from VDD to Vsp is given by

t2=Ctot*((Vdd-Vsp)/Id1)

The oscillation frequency of the current starved VCO for N (an odd number >= 5) number of stages is

Fosc = 1/(N*(t1+t2))

Substitute t1+t2 value in Fosc Equation

Fosc =Id/(Vdd*Ctot*N)

At maximum frequency,

Vmax = Vdd.

Since,

Fosc=1/Tand Iavg=Id

The average current output of VCO is

Iavg = (N*Vdd*Ctot)/(T) - (I)

Substituting the values frequency and current in (I)

Id = N*Vdd*Ctot*Fosc

Fosc = (Id)/(N*Vdd*Ctot) - (II)

Here,

Fosc = Oscillation Frequency of VCO
N = No of stages,
Vdd = Supply Voltage,
Ctot = Total Capacitance of inverter
Id = Drain Current and
Cox = Oxide Capacitance ()

For 45 nm Technology,

Id = 5.9*10^-3
Cox = (Eo*Er)/Tox
Eo = 8085*10^-18F/um^2
Er = 3.97
Cox = 8.78fF/um^2

Substitute these values in (I),

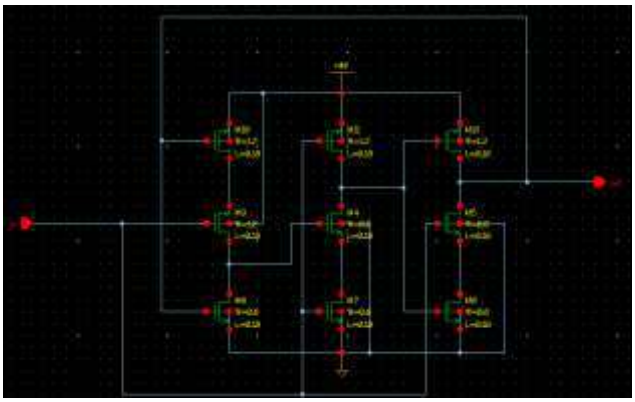
Ctot = (5/2)*Cox*(WpLp+WnLn)
Ctot = (5/2)*(8.784*Ff/μm^2)*((1μ*45n+1μ*45n)
Ctot = 19.75fF

Now substituting the values in (II)

Fosc = (Id)/(N*Vdd*Ctot)
Fosc = (5.9*10^-3)/(7*1.8*19.75*10^-15)
Fosc = 2.4 GHz

3.4 Frequency Divider

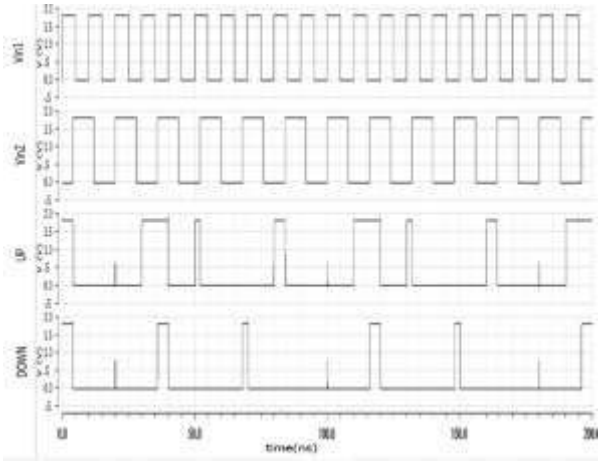
Frequency divider divides the VCO frequency to generate a frequency which is equal to reference frequency. We have used divide by 2 network, we can vary the divider network for synthesis of different frequencies. It divides the clock signal of VCO and generates D-clock which is applied to phase frequency detector which compare it with input data.



Schematic Diagram of Frequency Divider

3.5 Transient Response of PFD

Two pulse signals of different frequencies are connected with the inputs of Phase Frequency Detector, and resulting signals is observed at output terminals of PFD.

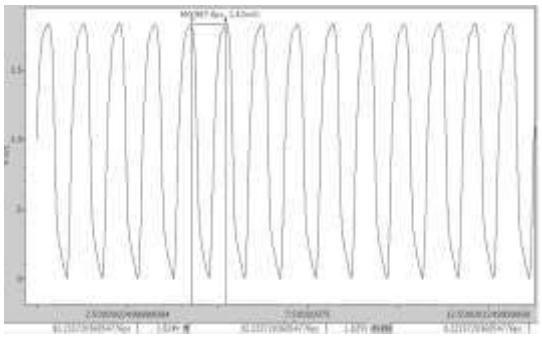


Transient Response of PFD

The phase of Vin1 signal leads the phase of Vin2 signal, UP will be HIGH, and when the phase of Vin2 signal leads the phase of Vin1 signal, DOWN will be HIGH.

3.6 Transient Response of Current starved VCO

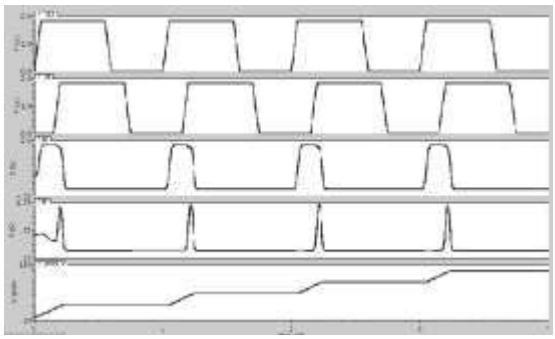
The main block of the PLL circuit is the voltage controlled oscillator. The circuit is designed to give a center frequency of 1 GHz. The center frequency of an oscillation at input control voltage is 1.05 GHz.



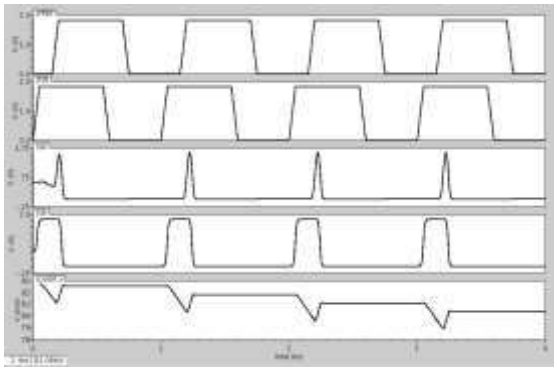
Transient response of Current Starved VCO

3.7 Transient Response of Charge-pump and LPF

In the below diagrams, the transient responses of charge pump during charging and discharging are shown.



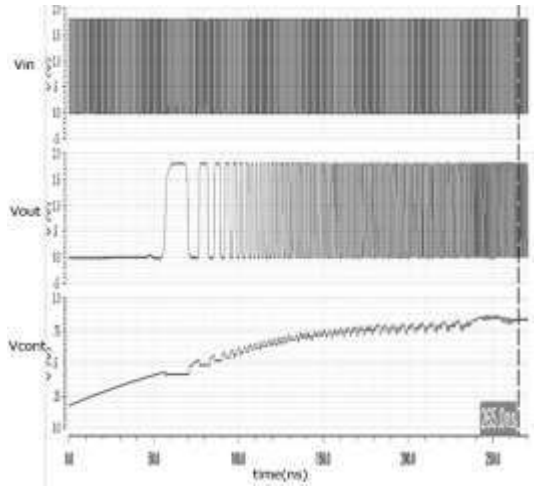
Simulation of Charge Pump (When Charging)



Simulation of Charge Pump (When Discharging)

4. TRANSIENT RESPONSE OF PLL

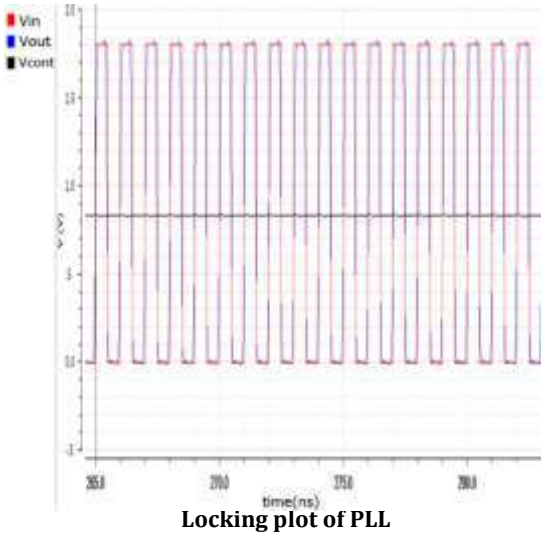
In the PLL, the control voltage starts increasing initially according to oscillation frequency, but after some time oscillations get sustained, and control voltage became constant and at this time locking starts. Locking range of the proposed PLL is 950MHz (50MHz – 1GHz).



Transient response of PLL

5. LOCKING PLOT OF PLL

In the below figure VCO output signal shows in blue, reference signal in red and control voltage in black. By overlapping them, it is clear that VCO output locked with input reference and control voltage is constant.



Locking plot of PLL

6. POWER DISSIPATION OF PLL

Total power dissipation is calculated as

$$P_{avg} = V_{dd} * I_{avg} = V_{dd} * I_{dd}$$

From the above expression,

P_{avg} is 277.2μW.

7. CONCLUSION

In the proposed paper PLL is implemented on CADENCE EDA 45nm process technology with an improved lock range 950MHz (50MHz–1 GHz)]. Proposed PFD is dead zone free and it has less area as compared to conventional PFD

due to absence of reset circuitry, also high gain 2.21GHz/V and larger tuning range 167MHz – 1.711GHz is achieved in designed CS-VCO. Simulation of this PLL circuit is done using spectre simulator of CADENCE and improved simulation results are obtained, i.e. power dissipation 277.2 μW and jitter 9.8ps at 1GHz.

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