ISSN (Online) : 2455 - 3662
SJIF Impact Factor :5.148

EPRA International Journal of

Multidisciplinary Research

Monthly Peer Reviewed & Indexed International Online Journal

Volume: 5 Issue: 3 March 2019

Published By :EPRA Publishing

Volume: 5 | Issue: 3 | March 2019 || SJIF Impact Factor: 5.148 ISSN (Online): 2455-3662

EPRA International Journal of
Multidisciplinary Research (IJMR) *Peer Reviewed Journal*

DESIGN OF CMOS BANDGAP VOLTAGE REFERENCE CIRCUIT

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ABSTRACT

This project implements the design of Bandgap reference circuit using the conventional method and the gm/ID method in CMOS 180nm technology. The circuit is designed, simulated and output voltage reference is found to be 1.2V at room temperature with the temperature range of -45°C to +125°C under a supply voltage of 1.8V. The BGR circuit is designed using two methodologies they are the traditional method and gm/ID method. The circuit was designed using Cadence Virtuoso schematic editor window and simulated using Spectre ADE. The bandgap reference circuit is used to provide a DC reference voltage that has little dependence on temperature variations. The important building block of many analog circuits is Temperature-independent references. They are commonly used in A/D and D/A converters, flash memories ,DRAMs as well as in variable gain amplifiers. In addition to the voltage stabilization over wide temperature ranges, there are errors introduced by process variations and power supply noise. The most widely used method for overcoming these challenges is bandgap reference circuit.

KEYWORDS— ***Bandgap voltage reference (BGR), PTAT-Proportional to absolute temperature, CTAT-Complimentary to absolute temperature, Temperature coefficient(TC).***

I. INTRODUCTION

In low-noise and low-jitter integrated circuits reference voltages, with high robustness against supply noise or temperature variations, are broadly demanded. Voltage references are important for ADC, DAC or memories and they are the essential part of every chip as the proper working conditions of the circuit needs some biasing. The voltage reference are required to be accurate and constant i.e. independent on temperature and supply voltage, preferably independent of the process and mismatch, low voltage and low power. It is hardly possible to design a circuit with ideal parameters and in most cases, temperature and supply voltage independence are preferred. These circuits can be useful for some applications due to their simplicity, despite poor voltage reference accuracy. Bandgap reference circuit is designed to produce a stable and precise output reference voltage which is independent of variations in Process, Voltage, and Temperature (PVT).

Based on the slope of variations through a wide temperature range, the temperature coefficient (TC) is either positive or negative. If both the positive and negative TC quantities participate in summation with proper proportion we can able to achieve a zero TC. For example, the base-emitter voltage of BJT transistor, V_{BE} and the thermal voltage (V_T), are known as negative and positive TC voltage terms respectively. Then, a zero TC voltage, V_{Ref} can be constructed by summing them.

II. PTAT CIRCUIT

The topology that provides PTAT TC is shown in Fig[1]. Assume that there are two identical NPN bipolar transistors Q1 and Q2, each one has a diff erent DC bias current. Their base and collector are connected and thus they behave like a diode. The simplified Shockley's equation is given by Eq.[3] it describes current through the diode and from the Eq.[3] Vbe is expressed by Eq.[4].

$$Ic = Is \cdot \exp(V_{be}/V_T) \quad (3)$$

$$V_{be} = kT/q \cdot \ln(Ic/Is) \quad (4)$$

Eq.[5,6] show voltage across these two BJTs

$$V_{be1} = V_T \cdot \ln(Ic1/Is) \quad (5)$$

$$V_{be2} = V_T \cdot \ln(Ic2/Is) \quad (6)$$

$$\Delta V_{be} = V_{be2} - V_{be1} = V_T \cdot \ln(Ic2/Ic1) \quad (7)$$

V_T is thermal voltage. Compare Equation 4,7 and it is evident that the expression is directly proportional to temperature i.e V_T = kT/q. Therefore ΔVbe is rising with temperature so it is known as PTAT circuit. The term ln(Ic2/Ic1) is a design choice of diff erent currents. The same circuit can be built with the same currents Ic1 = Ic2 and use diff erent area of PN junction. Or both principles together can be used, i.e. diff erent current and area.

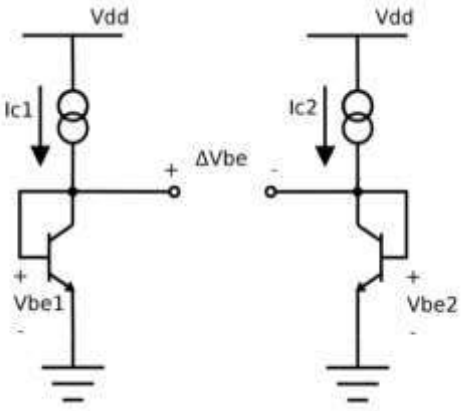

Figure 1: PTAT voltage realization

The PTAT circuit is shown in Fig[1] is simulated and the temperature behaviour is shown in Fig[2]

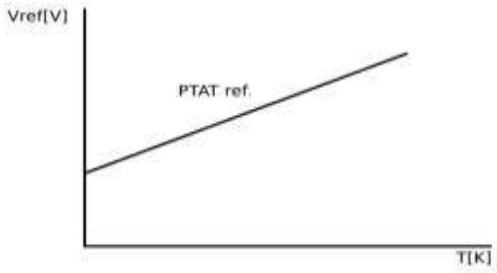

Figure 2: Graph of the PTAT circuit

III. CTAT CIRCUIT

A simple diode is used in order to generate CTAT circuit. NPN transistor shown in Fig.[5] has a base and collector connected which in turn act as diode that has two terminals. In this configuration, the base-emitter junction is exploited to obtain a diode. If a positive voltage is applied to pn junction, a forward biased region is entered. The relationship between I-V is approximated by Eq.[9] called Shockley's equation.

$$I = Is \cdot \exp(V/V_T) \quad (9)$$

V_T = thermal voltage, given by Eq.[10]
Is = saturation current

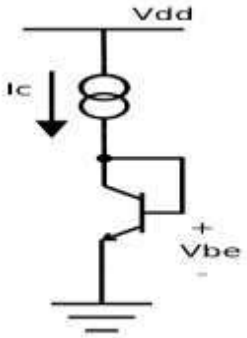

Figure 3: CTAT voltage realization

$$V_T = kT/q \approx 26mV/K \; T = 300K \quad (10)$$

where k = Boltzmann's constant = 1.38e-23 J/K
T = the absolute temperature in Kelvin
q = the magnitude of elementary electron charge = 1.60e-19 C
It can be derived,

$$\partial V_{be}/\partial T \sim = -2mV/K \quad (11)$$

The temperature behavior of diode connected bipolar transistor was simulated. The $\partial V_{be}/\partial T$ of NPN (180nm PDK) is −2.27mV/K at room temperature, the reference simulation result is shown in Fig.[4].

M

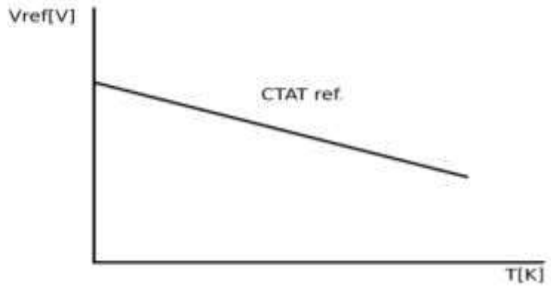

Figure 4: Graph of the CTAT circuit

IV. BANDGAP REFERENCE VOLTAGE

Bandgap reference (BGR) is used in both analog and digital circuits. It is an analog reference integrated circuit. In today's market, the ICs are being built to achieve higher integration and higher performance. Due to this trend the ICs have become complex and dependent on parameters such as temperature, supply voltage and process corners (TVP). The block diagram of BGR is shown in Fig[5]

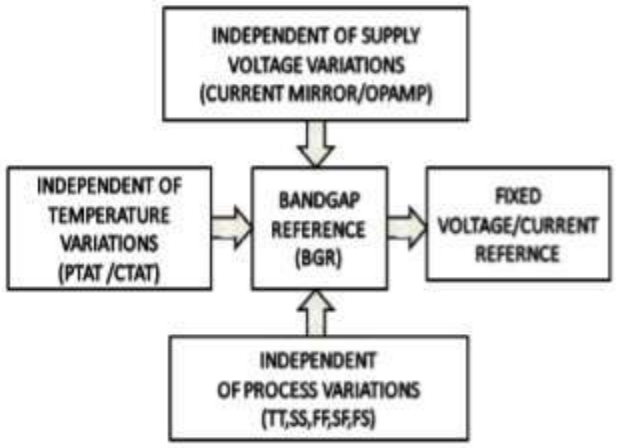

Figure 5: Block diagram of the Bandgap reference voltage circuit

A conventional bandgap reference is a circuit that performs summation of the forward-biased diode voltage having a negative temperature coefficient and a voltage proportional to absolute temperature (PTAT). As a consequence, controlled temperature dependent voltage close to the material bandgap of silicon(~1.22V) results. Voltage references obtained according to this approach are called bandgap reference(BGR) circuits.

As mentioned before, to compensate temperature dependence the BGR circuit is designed by exploiting CTAT and PTAT. The thermal voltage V_T = kT/q has a positive temperature coefficient (PTAT) and it rises by +85uV/K. Voltage base-emitter V_{be} has a negative temperature coefficient (CTAT) and its drop is about -2mV/K. Ideally, a zero TC is achieved by adding these two voltages, the simulation result of BGR is shown in Fig.[6]. It is evident that PTAT and CTAT are diff erent scales, therefore PTAT is multiplied by constant K to ensure their mutual compensation. Then the basic relation for BGR is

$$V_{REF} = m*V_{PTAT}(T)+n*V_{CTAT}(T). \quad (12)$$

Ideal means that output voltage V_{ref} has zero TC.

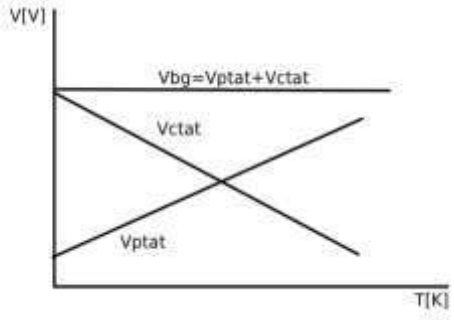

Figure 6: Zero TC due to PTAT and CTAT

V. DESIGN

The BGR design is given below

$$Vref = R2/R1\, ln(N)Vt + Vt\, ln(Io/Is) \quad (16)$$

$$Vref = \propto 1Vt + \propto 2VD \quad (17)$$

Slope of Vref =0 which implies $\frac{\partial Vref}{\partial T} = 0$

$$\propto 1\frac{\partial Vt}{\partial T} + \propto 2\frac{\partial VD}{\partial T} = 0 \quad (18)$$

By solving the equation with values $\frac{\partial Vt}{\partial T} = 85\mu V$

$\frac{\partial VD}{\partial T} = -1.6mV$ and α2=1, we get α1=18.82

$$I0 = \frac{Vtln(N)}{R1} \quad (19)$$

Where Io=5μA, V_T=26mV, N=2

Thus R1=3.6kΩ

$$\propto 1 = \frac{R2}{R1} ln(N) \quad (20)$$

Substituting the values we get R2=97.74kΩ

The basic circuit diagram with designed resistance values is shown in Fig [7].

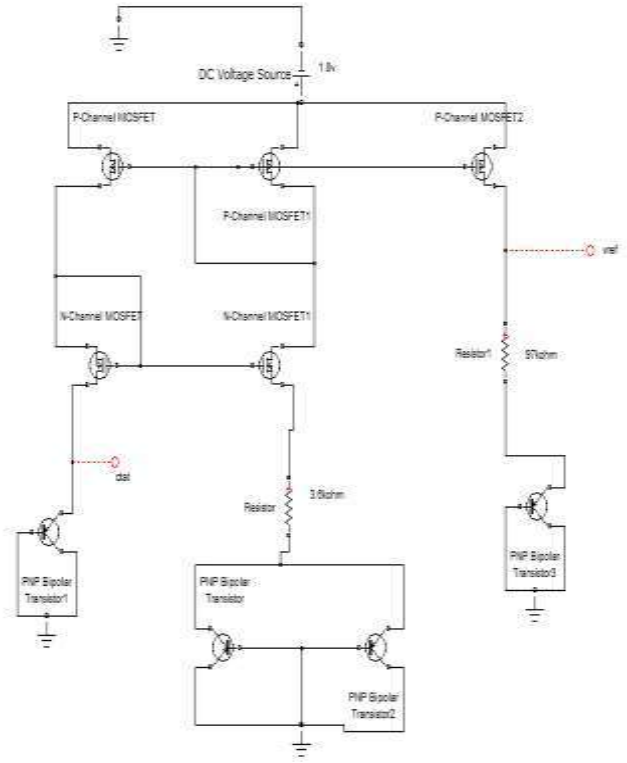

Figure 7: Circuit Diagram of BGR

VI. RESULTS

The circuits are designed using Cadence –Virtuoso Schematic Editor in 180nm CMOS technology. The circuits are simulated using Cadence Spectre and the results of the simulations are analyzed

The PTAT circuit with a current mirror for constant current supply is simulated it is shown in Fig [8].

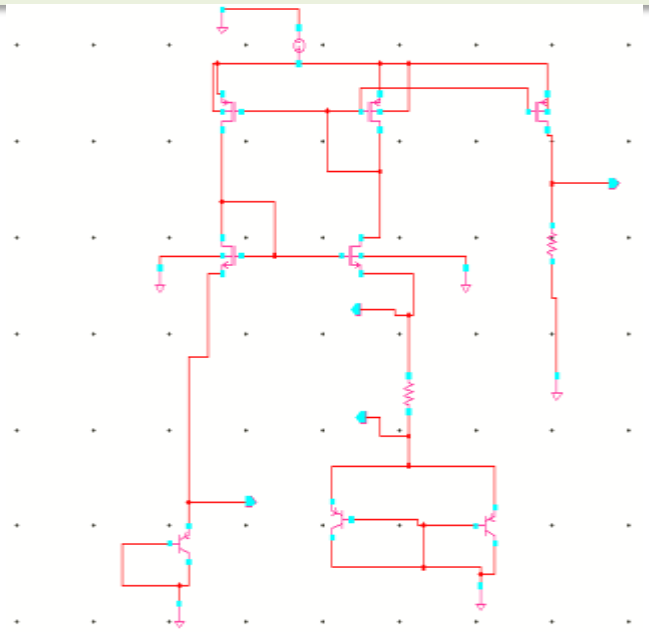

Figure 8: Simulation Diagram of PTAT

The simulated result of the PTAT circuit is shown in Fig [9], the output voltage is varying proportionally with respect to temperature.

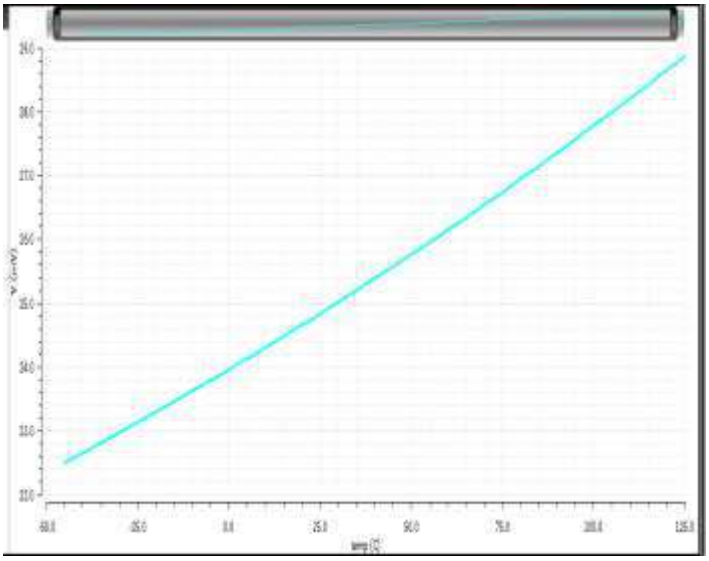

Figure 9: Simulation Results of PTAT

The CTAT circuit with a constant current source is simulated it is shown in Fig [10].
The simulated result of the CTAT circuit is shown in Fig [11], the output voltage is inversely proportional to absolute temperature.

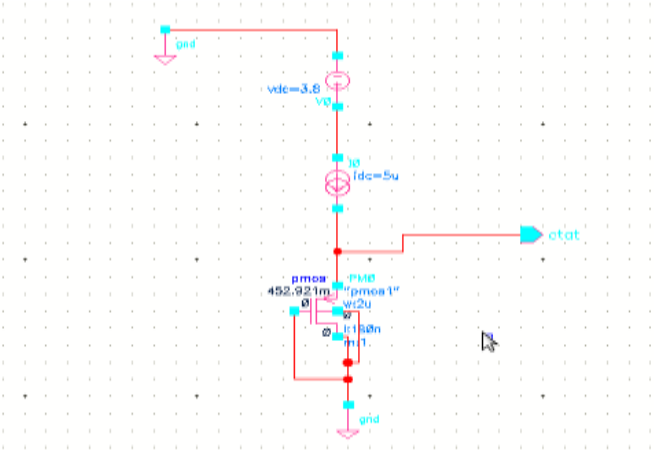

Figure 10: Simulation Diagram of CTAT

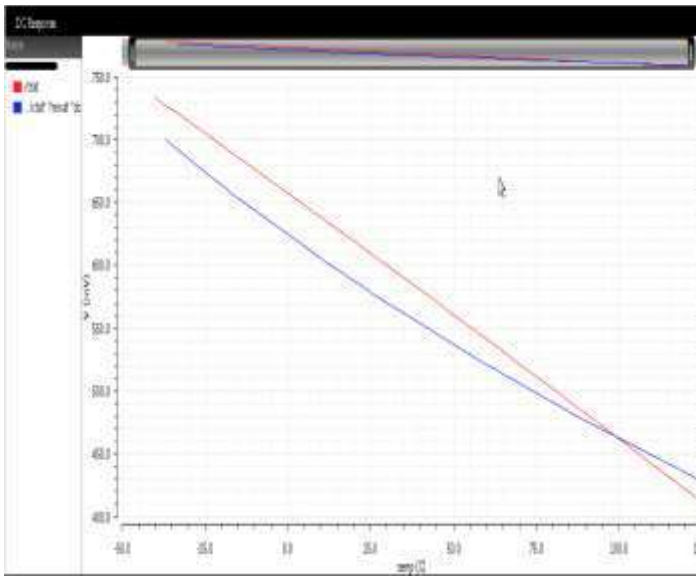

Figure 11: Simulation Results of CTAT

This BGR is built in the cadence environment and it is simulated for the temperature sweep it is shown in Fig[12]. The simulated result of BGR is shown in Fig[13], it is plotted for PTAT, CTAT and BGR voltages with respect to temperature

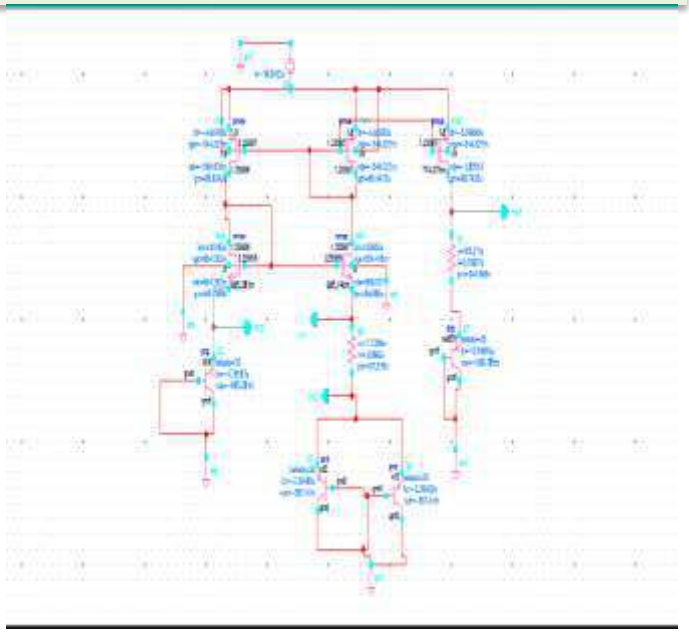

Figure 12: Simulation Diagram of BGR

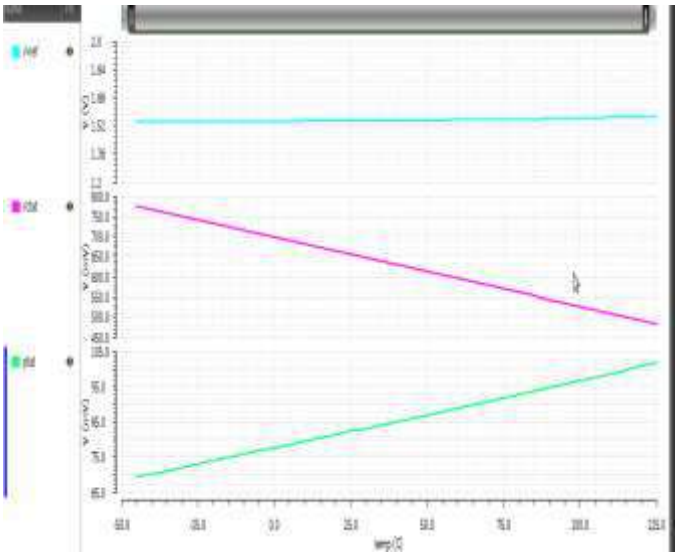

Figure 13: Simulation Results of BGR

The MOSFET is characterized using the gm/I_D, optimized for a specific width and the BGR circuit is designed. The designed BGR is simulated in the cadence virtuoso environment it is shown in Fig [14]. The designed BGR circuit is simulated by ADXL window for a range of temperature from -45^{o}c to +125^{o}c and the output waveform is shown in Fig [15].

Parameter	Traditional method	gm/I_D method
Supply Voltage	1.8v	1.8v
Output Voltage Range	1.53v-1.57v	1.23v-1.26v
Output Variations	40mv	30mv
Temperature Range	-45 to 125°c	-45 to 125°c

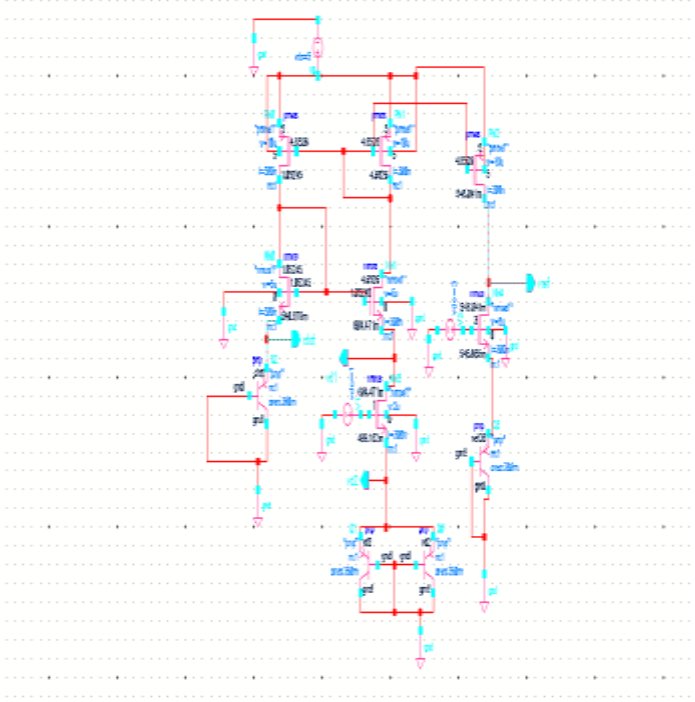

Figure 14: Simulation of gm/I_D BGR

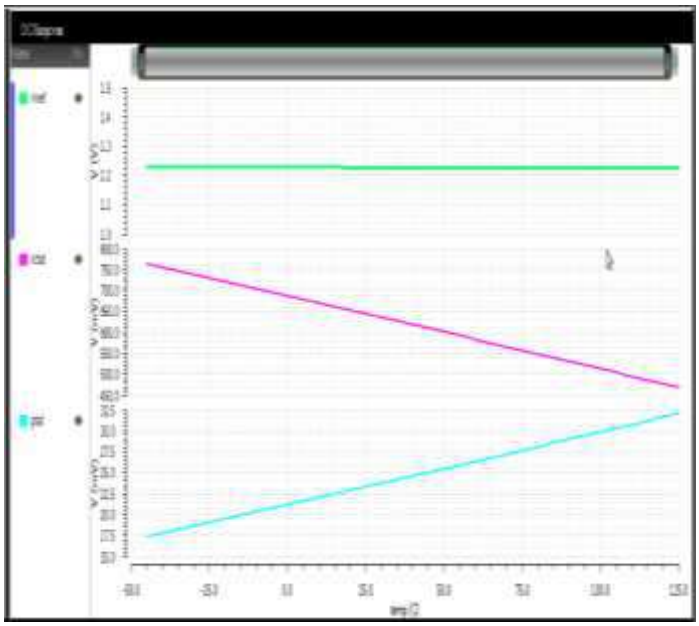

Figure 15: Simulation Results of BGR using gm/I_D

VII. Conclusion

A bandgap reference circuit that produces 1.22 V was presented. All the design specifications were met at nominal operating conditions and displayed over the design temperature range of -45°c to 125°c. The circuit is designed for operation with a 1.8V supply. Simulations also showed the circuit meets the design at most of the corners but could be improved in future work. The BGR is designed using the traditional method. The circuit was designed in the virtuoso schematic editor and simulated using ADXL window. The parameter analysis of the BGR circuit is achieved. The parameter analysis and comparison of traditional method and gm/I_D method is tabulated in the Table

Table: Parameter Analysis

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