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DESIGN AND IMPLEMENTATION OF FIVELEVEL SYMMETRIC INVERTER

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ABSTRACT

The design of five level inverter model using the available DC sources ,obtained from the external sources (e.g., a battery or a fuel cell stack)to produce five level sinusoidal output under the usage of Cascaded topology ,which accounts for several advantages over various other topologies in the inverter design .Thus resulting in five level output from symmetric inverter model being developed .

I. INTRODUCTION

Inverters are basically designed to meet out the basis needs of all the appliance requiring AC voltage sources as their input. In [1], a multilevel converter was presented in which the two separate DC sources were supplied to the two H-bridges in the cascaded connection. The main advantages of multilevel converters are low harmonic distortion of the generated output voltage, low electromagnetic emissions, high efficiency, the ability to operate at high voltages, and modularity [7]–[10]. In general, multilevel converters are categorized into diode-clamped [11]–[13], flying capacitor [14]–[16], and cascaded H-bridge multilevel topologies [17]–[20]In contrast, in this paper, hardware model is developed for the symmetric inverter using cascaded topology for five level and the output is obtained through DSO.The interest here is interfacing DC power sources on the PCB board developed and the connections made for cascade multilevel inverter , where the DC sources supplies both the auxiliary and the main H-bridges. As the name symmetric resembles the two voltages used in both H-bridges are equal. Currently, each phase of a cascade multilevel inverter requires n DC sources and this condition is verified through this paper. Thus the voltage levels of the DC sources are maintained and the output is expected to satisfy the fundamental frequency.

II. CASCADE MULTILEVEL INVERTER

A cascade multilevel inverter is a power electronic device built to synthesize a desired AC

voltage from several levels of DC voltages. Such inverters have been the subject of researchingthe last several years [2] - [6], where the DC levels were considered to be identical in that all of them, which were batteries, solar cells, etc. To operate a cascade multilevel inverter using DC sources, it is proposed to have two separate DC sources for the entire bridges with equal magnitude due to the symmetric condition.

There are several advantages for cascaded multilevel inverter over other topologies of the multilevel inverter connections which are listed as follows,

i)Elimination of excessively large number of bulky transformers

required by the multi-phase inverters.

ii)Avoidance of extra clamping diodes and flying capacitors which are

required by diode clamped and flying capacitors multilevel inverters.

iii) Simple and modular configuration.

iv) Flexibility in extending to higher number of levels.

Cascade multilevel inverters have been developed for electric utility

applications. Their applications are included as follows ,

i) Generate almost sinusoidal waveform voltage while only switching

one time per fundamental cycle.

ii) Dispense with multi-pulse inverter's transformers used in

conventional utility interface and static varcompensators.

iii) Enables direct parallel or series transformer-less connection tomedium-and high-voltage

.

The basic connections and the circuit diagram implementing the five level symmetric inverter model was shown in Fig. 1.It involves two H-bridges connected in cascaded topologies.The cascaeded connections resembles the same as that of in the series connection ,the only difference is that the output is feeded to the next H-bridges as input.But in the series conncetion ,the same input is feeded across all the components in the circuit.

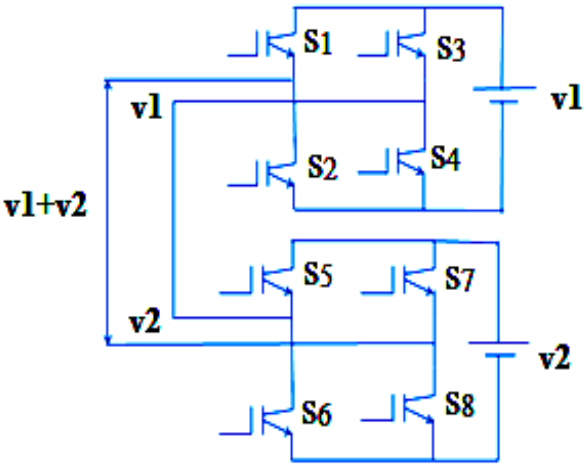

Fig. 1.Structure of a symmetric multilevel cascaded H-bridges inverter.

The DC source for the first H-bridge (H1) is a DC power source with an output voltage of Vdc, while the DC source for the second H-bridge (H2) is another voltage source tobe held at Vdc. Each H-bridges contains four switches and the produces respective output according to the triggering of it.The output voltage of the first and second H-bridges are denoted by v1and v2 respectively. The gross output from these two symmetric DC sourced cascade five level inverter is v = v1+v2. By opening and closing the switches of H1 appropriately, the output voltage v1 can be made equal to −Vdc, 0, or Vdc similarly ,the output voltage of H2 can also be made equal to −Vdc, 0, or Vdc by opening and closing its switches abruptly. Therefore, the output voltages of the inverter can have the values, −2Vdc, −Vdc, 0, Vdc, 2Vdc, which are the magnitudes of the five level output and is illustrated in Fig. 2. Table I shows how a waveform can be generated using the topology of Fig 1.(cascaded topology).Thus the switching operations containing the respective switches with their voltage magnitudes at each level are been cleared explained through the output waveform in Fig 2.,which was plotted against the time period (t) and magnitude of voltage in volts.The time is given by the reciprocal of the frequency i.e.,T=1/f,

Where f is the fundamental frequency of operation of the switches .

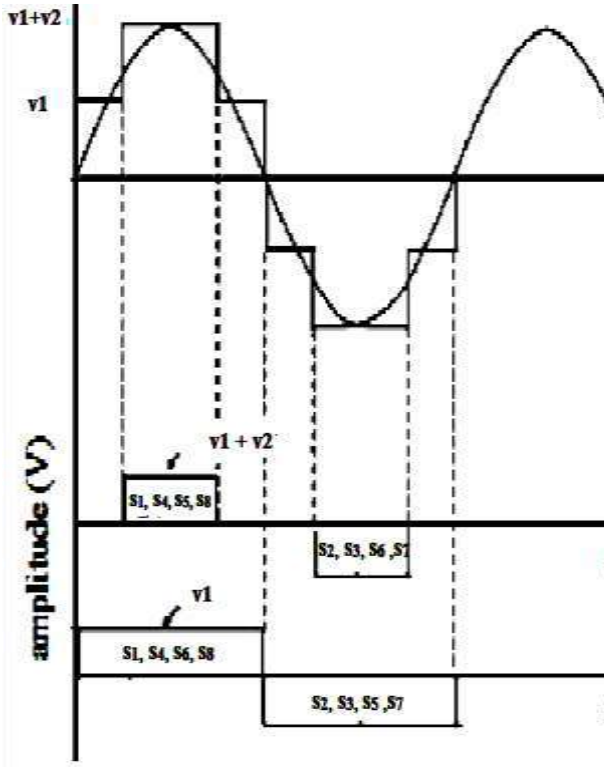

Fig. 2. Output waveform of 5-level symmetric cascade five inverter.

The voltage at main H-bridge ,v1 = Vdc is the voltage to be chosen. It is that v2=v1to be the voltage across the auxiliary bridge by the symmetric condition. The following Table 1 gives the switching conditions of the five level inverter model.

Switches	v1	v2	v =v1+v2
S_1,S_4,S_6,S_8	Vdc	0	Vdc
S_1,S_4,S_5,S_8	Vdc	Vdc	2Vdc
S_2,S_3,S_5,S_7	0	-Vdc	-Vdc
S_2,S_3,S_6,S_7	-Vdc	-Vdc	-2Vdc

Table 1.Switching conditions

III. SIMULATION MODEL

The simulation model is the pre-model circuit of the hardware to be developed through the MATLAB tool using the components available in it for analyzing the normal functioning of the circuit that has to be designed as a hardware. This paper deals about the design and implementation of symmetric five level inverter, which will be briefed in the following paragraphs.

IV. FIVE LEVEL INVERTER

The five level inverter model consisting of two H-bridges in cascaded connections, which are powered by two DC source for the main bridge and auxiliary H-bridge with the same magnitude, by the symmetric condition. The design of the circuit in MATLAB tool could be as shown in Fig 3, where each subsystem represents a H-bridge. Subsystem 1 is the main H-bridge with DC source of magnitude Vdc and the subsystem 2 is the auxiliary H-bridge with another DC source with the same magnitude. The load being used could be of resistor, since the simulation circuit could be grouped under the subsystem which involves the Simulink model to look simple and easily understandable.

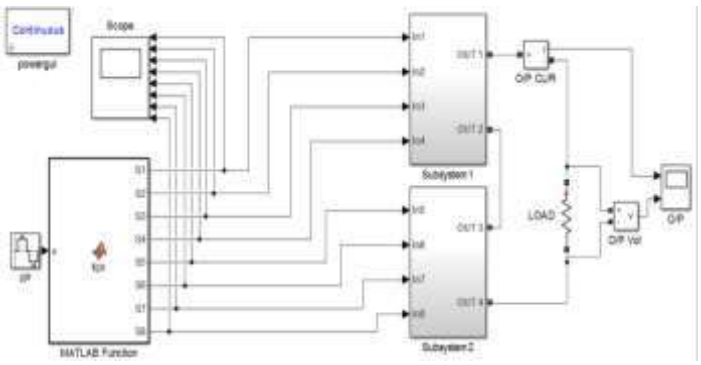

Fig. 3. Simulink model of symmetric five level inverter

V. MATLAB OPERATIONS

The switches used for the inverter operations are MOSFETs thet needs trigger pulse for its effective function. In order to provide the gate pulse, the MATLAB program was developed. It ensures control and effective operation of the inverter switches that were developed,thus enabling the switching of gate signals according to the program being developed for the proper functioning of the sewitches, contributing to the better performance of the inverter. In spite of using separate pulse generators across each switches, the MAT function enables the generation of same pulse through program which could be more effective and easy. Considering the effective use of normal pulse generator, which helps in the process of providing the gate pulse to the power electronic switcheswhich are more effective only for small circuits, where the pulse angle values should be changed for various operation of the switches .The calculation of those angles is possible for small circuits , but for a circuit with numerous power electronic switches which could be complicated to change the switching pulse angles at every stage of operation . Thus by the use of MAT function for programming which could be more robust and reliable ,thus reducing the complications of calculating the angle value at every interval of time.

VI. GATE PULSE

The switches thus being used in the H-bridge requires the external supply to the gate terminals. Since it is a gate controlled device. Thus these gate signals could be generated either by PWM or by using the MAT function (where the normal program could be made). Thus the gate signals are needed for triggering on the switches being used in the H-bridge circuit.For each switches,namely $S_1,S_2,S_3,S_4,S_5,S_6,S_7,S_8$ the gate signals should be given separately.The basic

common thing could be that ,all the gate pulse values are limited to 5V.Inorder to reduce the confusion in naming ,the switches arebeing named in the consecutive order starting from the main bridges then moving to auxillary bridges.Since MOSFET is voltage controlled device, gate voltage provides the necessary control process. Fig 4 shows the timing sequence at which the switches are triggered,which are generated by programming through the MAT function .

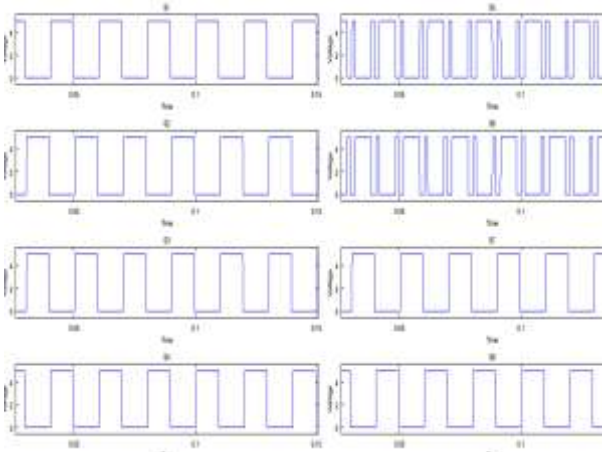

Fig. 4.Gate pulses of the switches using MAT function

VII. SIMULATION OUTPUT

The simulation model that results in the output which could be a symmetric five level waveform. This has been successfully arrived with theappropriate output voltage and current across the load resistor of 100Kohms(load value choosen).Thevoltage across the load could be similar as shown in Fig 5 determining the relation between time period and current.

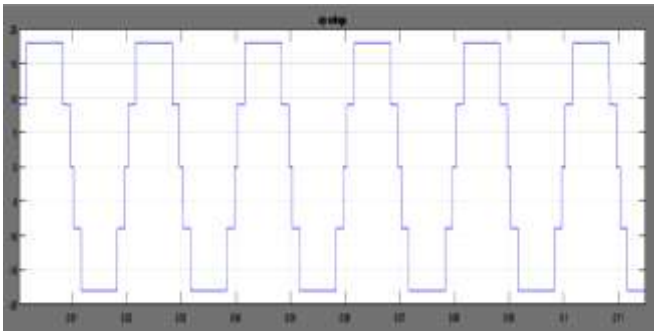

Fig. 5. Simulink output of voltage

The current drawn by the load could be similar as shown in Fig 6 which was plotted against time period and current.The current drawn could be varied depending upon the load requirements.Here the load is the resistor of value 100Kohms and so the corresponding current drawn was minimum.

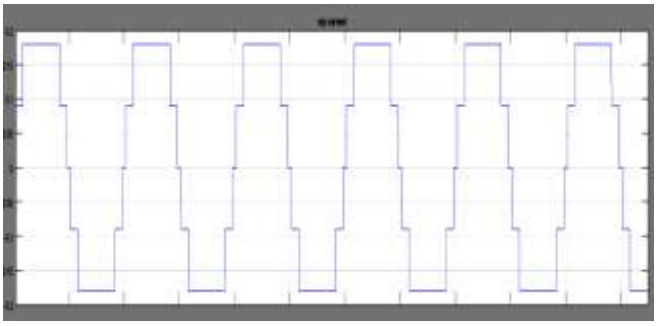

Fig .6. Simulink output of current

VIII. THD ANALYSIS

Total Harmonic Distortion of any system could be calculated which results in the harmonics level in that particular circuit. Thus in the MATLAB tool by using FFT analysis option the THD level in this simulation model of symmetric five level inverter has been obtained as shown in Fig 7and 8.Its very essential to verify the harmonics level of the circuit to find its efficient operation .As its important to reduce the harmonics level in the circuit is very important to make the circuit to work more effectively.

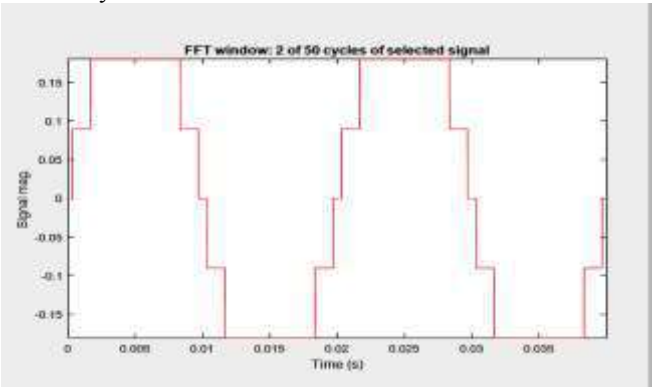

Fig. 7. FFT Analysis

The value of THD has been reduced compared to the three level inverter. Thus by increasing the levels of the output, the THD could also be reduced accounting for the improved efficiency.

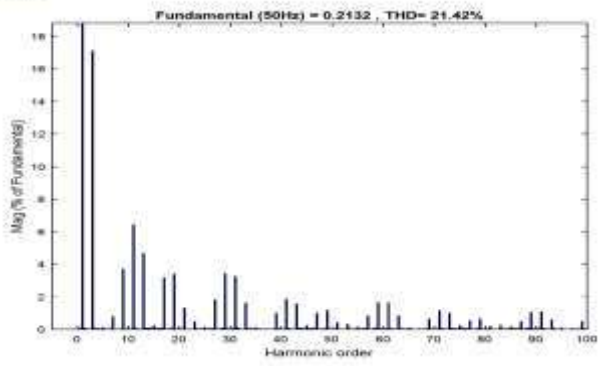

Fig.8 .THD Level

IX. HARDWARE MODEL

The hardware model is developed after the successful completion of the simulation model. Thus for the hardware development the components needed are as follows in the Table 2.

Table 2.Hardware components.

S.No	Name of the component	Range/Specification
1.	MOSFET	IRFP150N
2.	Driver	TLP250H
3.	Resistor	100 Ω
4.	Capacitor	400 µf
5.	Frequency	50HZ
6.	Main DC voltage	9V
7.	Auxiliary DC voltage	9V

The hardware model thus developed using these components and its working model is represented in the Fig 9.The hardware model thus developed through the eagle software ends with the PCB board. All the components mentioned above are placed over the appropriate places on the board along with the supply mains and the DC sources .The main operation could be the conversion of the fixed DC to the AC voltages through the usage of the MOSFET switches and the controller .All the MOSFET switches are being triggered by the signal from the controller .The controller receives the control signal from the MAT program an dit enables the gates of the respective switches which are being connected to the transformer for the trigger input .Once the gate of the respective switch receives the control signal ,it enables the supply to the switches which then make the process of forward/reverse bias according to the supply terminals.Thus all these ends up I supplying the load and the output is taken with the help of DSO .

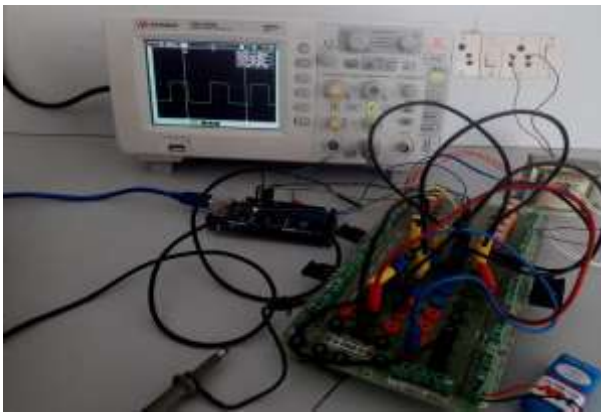

Fig. 9.Working model of symmetric five level cascaded inverter

The hardware model is being tested for its proper functioning and the output thus obtained are accurate and it is represented in Fig 10.Withan amplitude of 18V due to the combination of two symmetric voltages of 9V

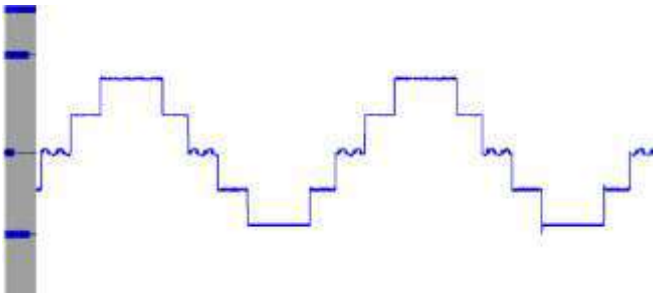

Fig. 10.HardwareOutput Voltage

X. CONCLUSION

The implementation of the cascaded five level symmetric inverter with its design , simulation model and hardware development was completed and the output was also been verified. Thusthe hardware output obtained could ensure the generation of the five level AC voltage with the symmetric DC voltages available and also the interest towards the implementation of increased levels of AC voltages from this inverter circuit, reducing the harmonics levels are some challenging actions in this inverter design which will be continued .

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