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SINGLE PHASE SHUNT ACTIVE POWER FILTER

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ABSTRACT

This paper proposes an single phase shunt active power filter, which eliminates harmonics drawn by nonlinear loads. Generally the peak voltage of an APF should be greater than the AC voltage at the point of common coupling(PCC) to ensure boost operation of the converter in order to inject harmonic current into the system effectively; therefore , full compensation can be obtained. The proposed modified PUC5(MPUC5) converter has two equally regulated separated DC links, which can operate at noload condition useful for APF application. Here the converter act as an filter. Those divided DC terminals amplitudes are added at the input of MPUC5 converter to be generate a boosted voltage that is higher than the PCC voltage. The voltage balancing unit is integrated into modulation technique to be decoupled from the APF controller.The proposed APF is tested to validate its good dynamic performance in harmonic elimination.

KEY WORDS: *Active Power Filter, PUC5, Harmonics Elimination.*

I. INTRODUCTION

APFs are currently installed on different spots to compensate the current harmonics and reactive power demanded by various nonlinear loads such as diode rectifiers, induction heating systems, electric arc furnace, etc. APF controlled by two methods. In direct mode, harmonic components of the load current are extracted and then sent to the controller as reference current. The indirect mode implies that the AC input current is synchronized with the utility voltage without using any harmonic extraction unit. This method is simpler since it requires only one controller to generate the reference signal, which is modulated to send the required pulses to the switch of the APF. Actually, in indirect control mode, the APF is considered as an active rectifier that its DC voltage and AC current should be controlled effectively.

.In this paper PUC5 converter is used as APF and the control circuit consists of a voltage controller, a resettable integrator, a comparator, an on-time doubler, a zero crossing detection circuit, and a bidirectional switch for the line current sensing. The control circuit and converter circuit are discussed briefly in the below.

II.PUC5 CONVERTER

Packed U-Cell(PUC) inverter has been first introduced by Al-Haddad et al. to generate seven-level voltage while using only six active switches, one isolated DC sources and one capacitor as second source which is voltage should be controlled to fix at 1/3 of first DC source. The PUC topology is investigated to have simple controller and better performance, which led to proposing a new self-voltage-balancing sensor-less five-level PUC inverter called sensor-less PUC5. The PUC5 inverter capacitor voltage would be fixed at half of the dc source amplitude using a self-voltage-balancing process which is integrated into the multicarrier Pulse Width Modulation (PWM). Therefore, there would be no necessity of using voltage or current sensors due to not using complicated controllers. Since the capacitor voltage is kept constant at desired level, the output voltage waveform would have symmetrical five levels with less harmonic distortion.

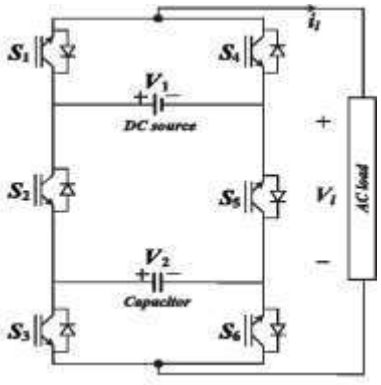

Fig.1 PUC5 Inverter Topology

MODE OF OPERATION

The single-phase PUC inverter topology has been shown in Fig.1. The complete associate switching states are listed in Table.1.

S	S1	S2	S3	S4	S5	S6	V_{out}	V_L
1	1	0	0	0	1	1	V1	+2 E
2	1	0	1	0	1	0	V1-V2	+E
3	1	1	0	0	0	1	V2	+E
4	1	1	1	0	0	0	0	0
5	0	0	0	1	1	1	0	0
6	0	0	1	1	1	0	-V2	-2E
7	0	1	0	1	0	1	V2-V1	-E
8	0	1	1	1	0	0	-V1	-E

Table.1 All possible switching states of PUC inverter

It is clear that eight existing switching states can provide different paths for current to flow through the system including dc sources and load. In PUC5 converter, the capacitor voltage should be 1/3 of the DC source magnitude (V_1). For instance, according to Fig 1, if $V_1 = 2E$, then V_2 should be regulated at E. Consequently, the five voltage level include 0, ±E, ±2E. Producing such high number of levels using only a single-DC-source inverter. The associated switching states have been listen in Table I. Assuming $V_1 = 2E$, the capacitor voltage should be regulated at half level so $V_2 = E$. It generates 5 voltage levels at the output while using a single DC-source. As seen in Table I, switching states of 2,3 and 6,7 generates same voltage level at the output using different paths. Those redundant switching states could be integrated into the modulation technique to balance the capacitor voltage at desire level. Moreover, having redundancy at zero voltage level helps reducing the switching frequency during transition between voltage levels of +E to 0 and 0 to +E.

The sensor-less voltage balancing technique has been proposed in which uses only one redundancy in switching states. Since it is free of sensing the capacitor voltage, there would be no control on the voltage ripple which forces to use very big capacitance at DC link.

In spite of the reported sensor-less voltage control on the PUC5 inverter, a voltage sensor could be added to the inverter box as a feedback to the voltage controller block and then the redundant switching states would be involved in regulating the capacitor voltage at desired level. The PUC5 inverter not only generates 5-level voltage waveform and it also reduce the harmonics.

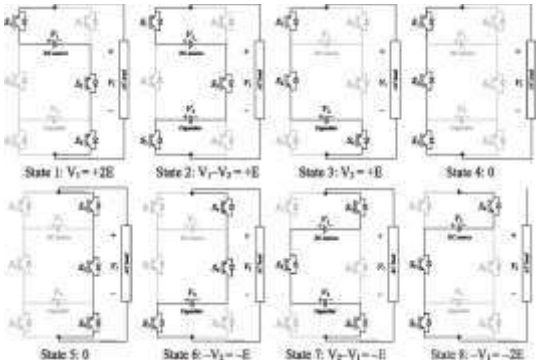

Fig 2.Switching States and Conducting Paths of PUC5 inverter

The capacitor charging and discharging time only depends on load value. Larger loads need smaller capacitor in dc link and vice versa. This self-voltage-balancing procedure can be mathematically proved based on capacitor energy relations. Fig 3. shows one cycle of the typical output voltage and current waveforms of PUC5 inverter. *VE* is a part of output voltage generated by the capacitor (*±E* or *−E*) whether connected to the load alone as discharging path or in series with dc source as charging process.

STATE	CAPACITOR VOLTAGE
1	No effect
2	Charging
3	Discharging
4	No effect
5	No effect
6	Discharging
7	Charging
8	No effect

Table 2. Capacitor Voltage States

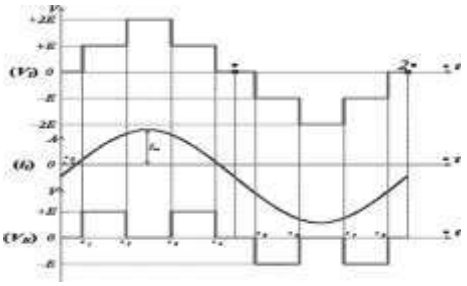

Fig 3. Typical output voltage and current waveform of five level inverter

III.PHASE LOCKED LOOP

A phase-locked loop is a control system that generates an output signal whose phase is related to the phase of an input signal. There are several different types; the simplest is an electronic circuit consisting of a variable frequency oscillator and a phase detector in a feedback loop. The oscillator generates a periodic signal, and the phase detector compares the phase of that signal with the phase of the input periodic signal, adjusting the oscillator to keep the phases matched. The simplest analog Phase Locked Loop is shown in Fig 4.

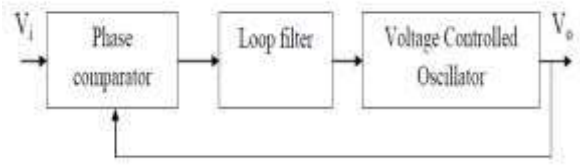

Fig 4 Simplest analog phase locked loop

Keeping the input and output phase in lock step also implies keeping the input and output frequencies the same. Consequently in addition to synchronizing signals, a phase-locked loop can track an input frequency, or it can generate a frequency that is a multiple of the input frequency. These properties are used for computer clock synchronization, demodulation, and frequency synthesis.

Phase-locked loops are widely employed in radio, telecommunications, computers and other electronic applications. They can be used to demodulate a signal, recover a signal from a noisy communication channel, generate a stable frequency at multiples of an input frequency (frequency synthesis), or distribute precisely timed clock pulses in digital logic circuits such as microprocessors. Since a single integrated circuit can provide a complete phase-locked loop building block, the technique is widely used in modern electronic devices, with output frequencies from a fraction of a hertz up to many gigahertz. General block diagram of Phase Locked Loop is shown Fig 5.

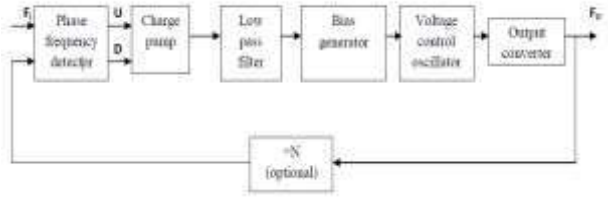

Fig 5 Block diagram of PLL

A phase detector compares two input signals and produces an error signal which is proportional to their phase difference. The error signal is then low-pass filtered and used to drive a VCO which creates an output phase. The output is fed through an optional divider back to the input of the system, producing negative feedback loop. If the output phase drifts, the error signal will increase, driving the VCO phase in the opposite direction so as to reduce the error. Thus the output phase is locked to the phase at the other input. This input is called the reference.

Analog phase locked loops are generally built with an analog phase detector, low pass filter and VCO placed in a negative feedback configuration. A digital phase locked loop uses a digital phase detector; it may also have a divider in the feedback path or in the reference path, or both, in order to make the PLL's output signal frequency a rational multiple of the reference frequency. A non-integer multiple of the reference frequency can also be created by replacing the simple divide-by-*N* counter in the feedback path with a programmable pulse swallowing counter. This technique is usually referred to as a fractional-N synthesizer or fractional-N PLL.

The oscillator generates a periodic output signal. Assume that initially the oscillator is at nearly the same frequency as the reference signal. If the phase from the oscillator falls behind that of the reference, the phase detector changes the control voltage of the oscillator so that it speeds up. Likewise, if the phase creeps ahead of the reference, the phase detector changes the control voltage to slow down the oscillator. Since initially the oscillator may be far from the reference frequency, practical phase detectors may also respond to frequency differences, so as to increase the lock-in range of allowable input.

PI CONTROLLER

A variation of Proportional Integral Derivative (PID) control is to use only the proportional and integral terms as PI control. The PI controller is the most than full PID controllers.

The value of the controller output u(t) is fed into the system as the manipulated variable output.

DISCRETE PI CONTROLLER

Digital controllers are implemented with discrete sampling periods and a discrete form of the PI equation is needed to approximate the integral of the error. This modification replaces the continuous form of the integral with a summation of the error and the uses Δt as the time between sampling instances and n_t as the number of sampling instances.

$$u(t) = u_{bias}+K_ce(t)+K_c/TI(i=1\Sigma ntei(t)\ \Delta t) \qquad (3.2)$$

where,
K_c=Controller Gain
TI=Integral time constant
Δt=Time between sampling instances

PI control is needed for non-integrating processes, meaning any process that eventually returns to the same output given the same set of inputs and disturbances. A p-only controller is best suited to integrating processes. Integral action is used to remove offset and can be thought of as an adjustable u_{bias}.

IV. SIMULATION AND RESULT

The block diagram of Shunt Active filter is shown in below Fig 6

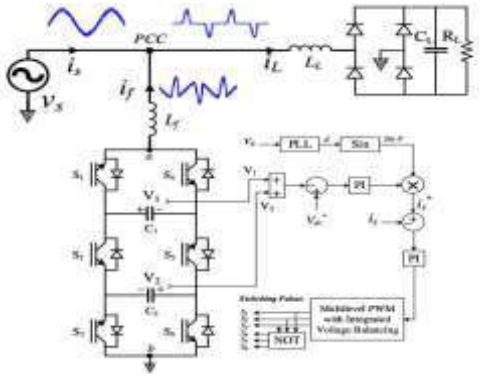

Fig 6. PUC5 APF connected to the AC source and nonlinear load

By applying KCL at the Point of Common Coupling(PCC), the sum of source current and filter current is equal to the load current.

$$I_S + I_F = I_L$$

Where,
I_S = Source current
I_F = Filter current
I_L = load current

When the system is connected without a filter the value of I_F and hence the value of source current is equal to the value of load current. (i.e.,) $I_S = I_L$. in the absence of the filter the harmonic in the load will also affect the source current. Hence the source current will also be non sinusoidal in nature. This is shown in the fig 7 & 8 given below

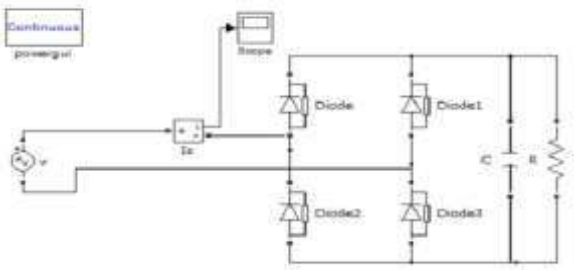

Fig.7 Non linear load without filter

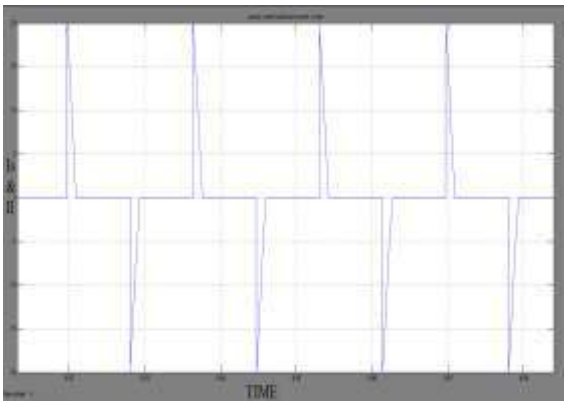

Fig 8. Source current V_s load current

To reduce the harmonics, filter is added at PCC. The filter injects anti-harmonic signal which is used to eliminate the harmonics present in the source current. Thus after insertion of the filter at PCC the source current becomes sinusoidal and the harmonics is compensated. The result is shown below fig 9.

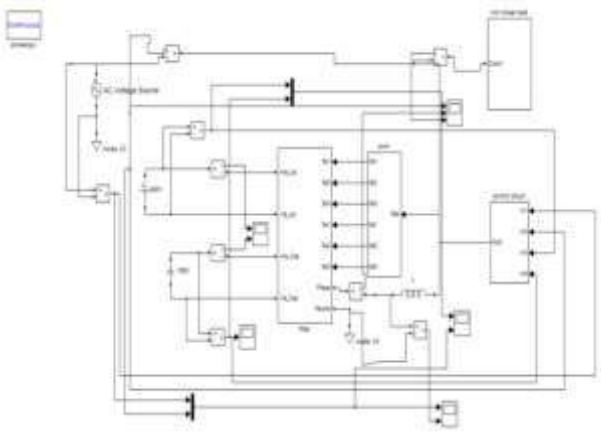

Fig 9. Simulation of Shunt Active Power Filter

In the below fig 10, after inserting the filter at PCC the harmonics in the source current in

reduced and it is transferred to the sinusoidal waveform.

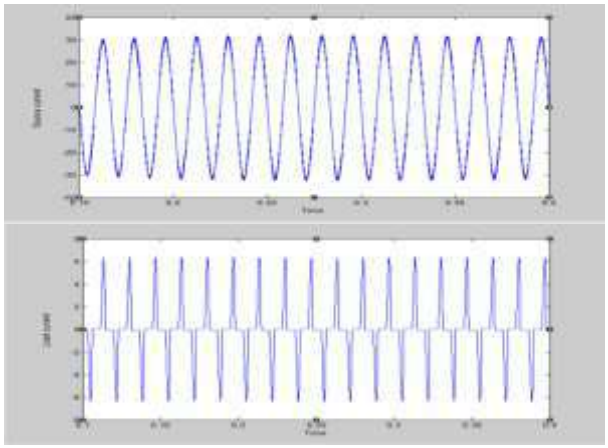

Fig 10. Source and load current after connecting filter

Load current is non sinusoidal as it is affected by harmonics but due to the antiharmonics injected at the PCC the source current become sinusoidal.

The harmonic distortion before the connection of filter at PCC will be 72%. When the filter is connected at PCC the value of harmonic distortion is reduced to 2%. The graph shows the value of harmonic distortion before and after connecting filter.

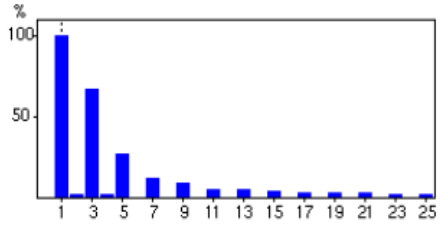

Fig 11.THD spectrum before using filter

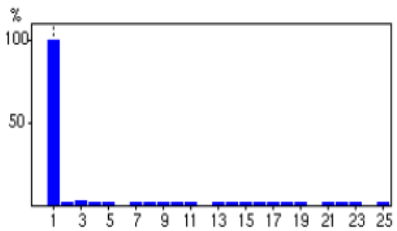

Fig 12. THD spectrum after using filter

V. CONCLUSION

Shunt Active Power Filter is designed using MATLAB simulink file and its output is evaluated. In absence of Filter, the source current is same as the load current which is affected by harmonics. When filter is added at the Point of Common Coupling it injects anti-harmonics signal to eliminate the harmonics in the source current is. Thus the harmonics is eliminated at the source current and the output is verified. The harmonics is reduced from 72% to 2% when the active filter is added at PCC. Thus the harmonics is reduced and the system will be protected by using shunt active power filter.

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