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## IMPROVED LATENCY SYNCHRONIZER PERFORMANCE USING SEQUENCED LATCHING

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### ABSTRACT

*In synchronization of sequential circuit, the random variation in input signal can cause the unwanted transition at output node. To check these transitions, different supply voltages with variable frequencies are applied to these sequential circuits. The unwanted transition at output nodes leads to the metastability. This is the unwanted state lie between the logic level '1' and logic level '0'. In this work a microwind and DSCHE layout simulator is used to design the latches and flip flops and to estimate the parametric analysis such as power dissipation, rise time and fall time switching delay, total number of transistors required for design, data frequency and clock frequencies etc.*

**KEYWORDS:** microwind, flip flops, circuit, trigger clock signal

### I. INTRODUCTION

The flip flop based synchronized sequential circuit shows the best performance against metastability. This metastability occurs at the violation of setup and hold time of flip flop circuit. The metastability can be reduced by re-sampling the input signal through synchronized flip flops. This will increase the latency as it takes several times to resolve the valid logic state at output node. This can also be avoided by designing the improved switching time such as rise time and fall time MOSFET circuit's base flip flops. Ways of limiting metastability include using only one clock, using faster flip-flops, and decreasing the asynchronous input frequency, and using synchronization hardware. These steps can easily be taken by designers to increase the reliability of a circuit. The edge-triggered flip flops are designed with master and slave connected latches. The propagation delay of flip flop circuit depends on the switching delay and propagation delays of master and slave latch. The

synchronization of flip flops follows the fundamental mode of operation which states the input change time should be at least equal to or greater than the propagation delay of entire synchronous sequential circuits. If any of the flip flops in synchronized cascaded flip flops enters in metastable state will cause the metastability to propagate from one flip-flop to another. If this synchronized circuit having important state information then system may transition from wrong and non-recoverable state.

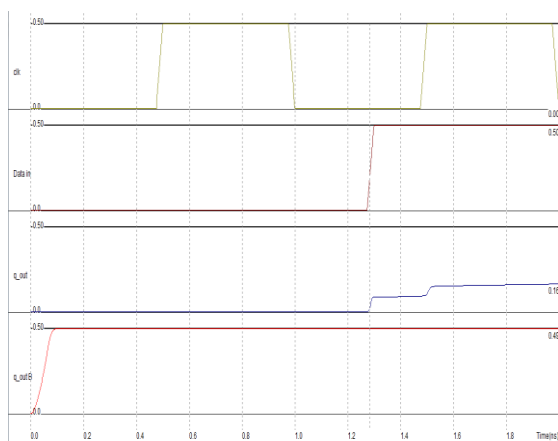
### II. RELATED WORK REVIEW

The synchronization latency for 8-bit counter, multiplier, finite state machine, shift register is simulated in [1]. The design trade-offs of flip flop for metastability failure, error detector and soft error robustness is discussed. The synchronization failure due to faults like metastability is avoided by using lower time constant flip flops. The flip flops were fabricated in

the nanometer range process and radiation measurements were performed at several test facilities. In their paper, a total of four flip-flops are considered for analysis. The first flip-flop is a standard master slave flip-flop [MS-DFF], which is used as a reference flip-flop. The second flip-flop [MS-Quatro, ] replaces the master and slave storage cells with the Quatro cell. The third and fourth flip-flops have only the slave stage protected, in one case with the DICE cell [S-DICE] and in the other case with the Quatro cell [S-Quatro, [1]]. In [2] the first flip-flop is a standard master slave flip-flop [MS-DFF], which is used as a reference flip-flop. The second flip-flop [MS-Quatro,] replaces the master and slave storage cells with the Quatro cell. The third and fourth flip-flops have only the slave stage protected, in one case with the DICE cell [S-DICE] and in the other case with the Quatro cell [S-Quatro,] [2]. By design the flip flops with different transmission gates, a multiplicity of flip-flops can be designed. The transmission gate provides a means for controlling the transfer of data into the memory cells while the memory cell stores the data after the transmission gate is deactivate [3, 4, and 5].

**III. TIMING METRICS**

The propagation delay between clock signals to output Q of flip flop is the sum of propagation delay of master latch and slave latch. If the output node of master latch enters in metastable state then the large time is require to settle the output node of master latch to a valid state. This will increase the propagation delay of flip flop. The flip flops are synchronized in such a way that output node gets sufficient time to settle to a valid logic level. The timing metrics of flip flop includes setup time and hold time.



**Fig 1.1 Flip-flop waveforms in the case of stable and metastable outputs**

**IV. PROPAGATION DELAY**

The propagation delay is the time required for the output to respond the changes on input after the activation of clock edge. The clock edge is either positive or negative.

**V. SETUP TIME**

After the activation of edge trigger clock signal, the input data must remain stable for a time interval so that flip flop will ensure the valid output level. This time interval is called as set uptime of flip flop.

**VI. HOLD TIME**

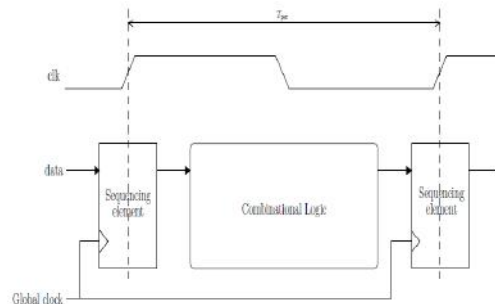
After the activation of edge trigger clock signal, the input data must be hold for a time interval so that flip flop will ensure the valid output level. This time interval is called as hold time of flip flop.

**VII. TOTAL DELAY**

The delay of a flip-flop can be defined as the time require from the variation in input to the variation at output. The total delay summation of setup time, hold time and delay time.

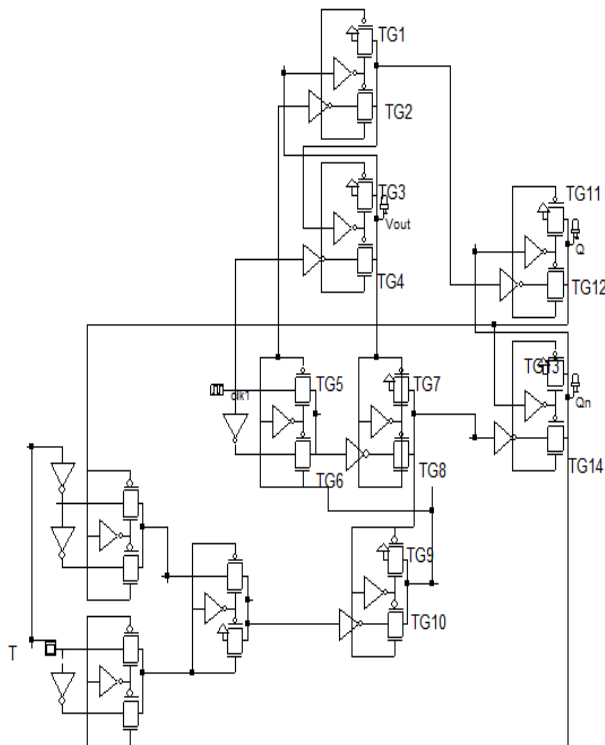
**VIII. SYNCHRONOUS SEQUENCING CIRCUIT**

The latch and flip flops are the basic synchronizing sequential circuits. Latches are transparent i.e. input changes flows directly through to the output node, while flip-flops are not transparent at any time when the clock signal level activates.



**Fig 2 Synchronous Sequencing Circuit:**

In delay flip flop the input data is transferred to the output node after one clock cycle. Hence this flip flop is called as delay flip flop. The characteristics equation of delay flip-flop can be given as:  
 $Q_{t+1} = D_{in}$   
 where  $Q_{t+1}$  is the output value in the next clock period and D is the input value sampled at the rising edge of the clock signal for the start of the clock period.



**Fig: Flip Flop Circuit.**

The T (toggle) flip-flop is a complementing flip-flop and can be obtained from a JK flip-flop when inputs J and K are tied together. When T = 0 (J = K = 0), a clock edge does not change the output. When T = 1 (J = K = 1), a clock edge complements the output. The complementing flip-flop is useful for designing

Binary counters.

The T flip-flop can be constructed with a D flip-flop and an exclusive-OR gate as shown in Fig. 5.13 (b). The expression for the D input is

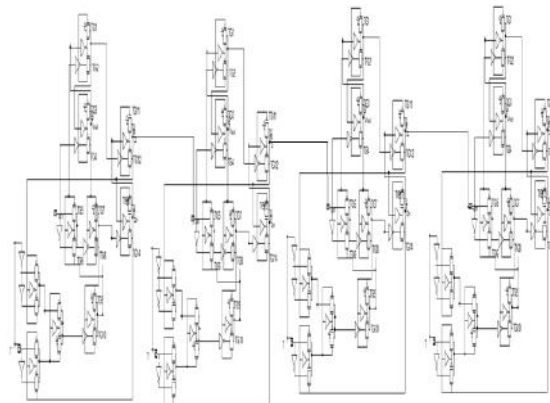
$$D = TQ_n + T_nQ$$

When T = 0, D = Q and there is no change in the output. When T = 1, D = Qn and the output complements. The graphic symbol for this flip-flop has a T symbol in the input.

**IX. SEQUENTIAL COUNTER CIRCUIT**

A Schematic design of four bit counter using edge trigger Toggle flip-flop is shown in fig ..... The counter circuit counts in a predefined sequence of states depends on the edge of clock signal. This clock signal may be generated from some other circuitry or through a clock pulse generator. For the n number of flip flops this counter counts maximum 2n-1 states. The fig shows the counter design using the three cross connected NAND gates design using transmission gates arrangement of toggle flip flops. The first two cross connected NAND gates latch generates the edge trigger clock pulse and the third cross connected NAND gate serve as a transparent Latch. Here the complemented output of D flip flop is

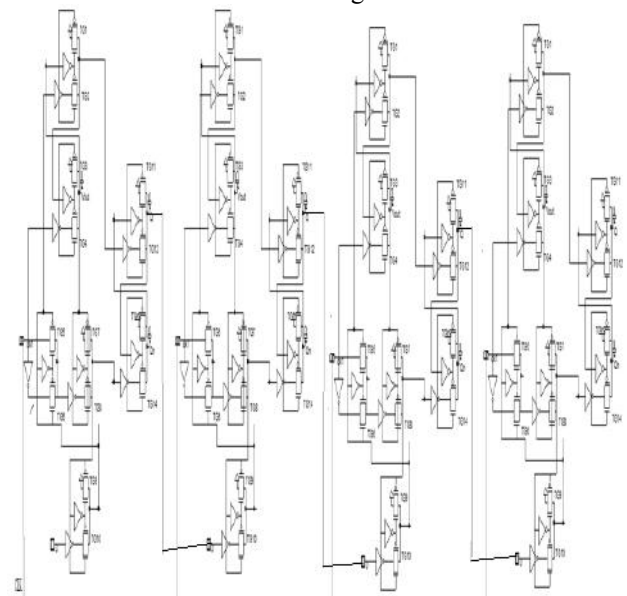
connected to the D input to design the Toggle flip flop. It consists of four flip flops design. Each flip flop consist of 14 transmission gates and 14 NOT logic gates comprises of 28 NMOS and 28 PMOS which is less than the number of transistors of conventional four bit asynchronous counter design. The conventional counter is design with 72 NMOS and 72 PMOS transistors.



**Fig Four bit sequential counter Schematic.**

**X. SYNCHRONIZED SHIFT REGISTER REGISTER**

A shift register consist of series connected flip flops without put of one flip flop is connected to the input of next flip flop. All the flip flops are synchronized with the same clock pulse. The latency of the shift register depends on the propagation delay of each flip flops and the applied clock frequency. At initial stage all the flip flops are reset by reset signal. The input which is to be shifted is applied on D input of first flip flop. At every edge trigger of clock pulse the data available at input port of each flip flop is transfer to the output node. As all flip flops are series connected this data is shifted from left to right direction.



**Fig Sequential Shift Register:**

The output is comes out serially from last flip flop. This shifting operation is also controlled by multiple clock pulses.

## XI. CONCLUSION

The synchronization failure due to faults like metastability can be reduce by using faster flip flop design or by ensuring a long enough clock periods so that the flip flop enters in quasi-stable states. Using faster flip-flops decreases the setup and hold times of the flip-flop, which results in decreases of the time window that the flip flop is susceptible to synchronization failure. When the input frequency reduces, the probability of the input changes during the setup and hold time also reduces.

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