ISSN (Online) : 2455 - 3662
SJIF Impact Factor :3.967

EPRA International Journal of

Multidisciplinary Research

Monthly Peer Reviewed & Indexed International Online Journal

Volume: 2 Issue: 12 December 2016

Published By : EPRA Journals

EPRA International Journal of Multidisciplinary Research (IJMR) ISSN (Online): 2455-3662

SJIF Impact Factor: 3.967 Volume: 2 | Issue: 12 |December 2016

DUAL DIABETICS CHOLESTEROL CALIBRATING APPLICATIONS BASED ON FIELD PROGRAMMABLE GATE ARRAY PLATFORM

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ABSTRACT

In this paper, a dual glucose/cholesterol meterapplication based on FPGA platform is introduced. It consists of a dual glucose/cholesterol readout circuit, an analog to digital converter (ADC), a digital controller, a serial Electrically Erasable Programmable Read-Only Memory (EEPROM), and a Liquid Crystal Display (LCD). The readout circuit is used to proportionally transfer the current signal detected by a glucose/cholesterol sensor. It was fabricated by 0.35 μm TSMC CMOS process with an area of 0.086 mm² and 409.29μW power consumption. The ADC is added to transfer the output signal of the readout chip in analog format to the input signal of the micro controller in the digital format. The digital controller is simulated by using a Field Programmable Gate Array (FPGA) as a platform, which displays the measured result on LCD and stores the detected data into the serial EEPROM. The linearity of this work is 0.9850 for the current sensing range of 5.01~22.3 μ A within glucose concentration range of 50~400 mg/dL with the power consumption of this system is 46.893 mW and current sensing range of 500~600 μA within cholesterol concentration range of 150~300 mg/dL. In addition, this system can produce the glucose concentration (mg/dL) results within 11 seconds which is faster than current products and previous works [1], [2] and the cholesterol concentration (mg/dL) results within 20 seconds. Compared to previous systems, the experiment results show that this work has a better performance in terms of linearity, accuracy and power consumption.

KEYWORDS: *Dual Glucose/Cholesterol Sensing System, Linear Current-Mode Readout Circuit, FPGA, Glucose sensing, Cholesterol sensing, Amperometric chemical sensor.*

I. INTRODUCTION

The increasing prevalence of cardiovascular diseases (CVDs) and diabetes mellitus has become serious public health issues nowadays. People with diabetes are two to four times more likely to develop CVDs compared to people without the conditions[3]. Thus, fast, effective and inexpensive cholesterol and glucose detection schemes are needed[4]. A dual glucose/cholesterol meter is a medical device for measuring levels of glucose and cholesterol concentration in the blood.

Therefore, the research for developing biosensor to monitor the blood glucose and cholesterol levels becomes very important in order to help people suffering with CVDs and diabetes mellitus. Several studies concerning glucose sensing systems have been presented recently.

Lai [2] presented a portable bio-sensing system by using ATMEGA 16L to process the signal. In addition, personal computers with the National Instrument Data Acquisition (NI DAQ) for developing glucose detection system is presented in [1]. However, the power consumption of personal computers is not suitable for a portable glucose sensing system.

Hence, a dual glucose/cholesterol sensing system by the VLSI technique is proposed in this paper. The signal can be processed faster and more reliably by using Altera DE2-115 FPGA platform. Furthermore, the performance and power consumption of the proposed system can be reduced by a cell based VLSI design. In addition, the gate count and power consumption can be reduced. Moreover, a serial EEPROM is used to store the data. Later on, the user can read the data log to track the glucose/cholesterol measurement for a certain period of time.

II. SYSTEM FEATURES

Fig. 1 shows the architecture of the proposed a dual glucose/cholesterol meter application based on FPGA platform, which compromises a dual glucose/cholesterol sensor readout circuit with a potentiostat, a 12-bit RC Hybrid Successive Approximation Register (SAR) type ADC, a digital controller unit (ASIC design controller), a LCD, and a serial EEPROM.

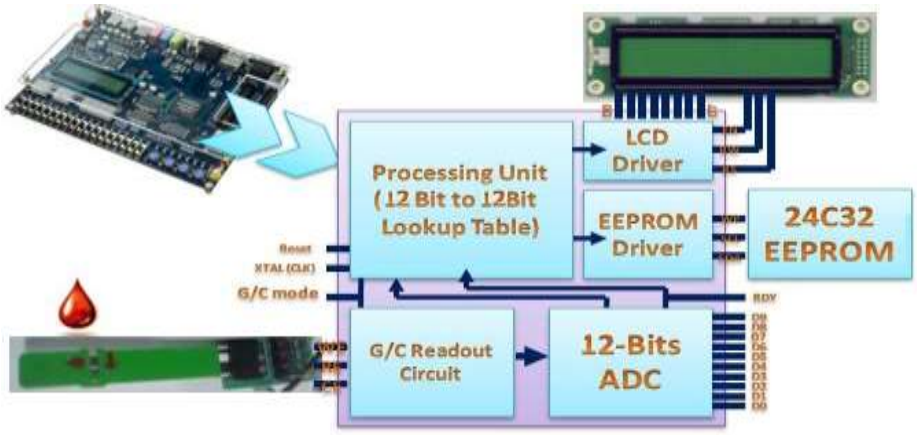

Fig. 1. Architecture of dual glucose/cholesterol sensing system

The readout circuit uses an amperometric method for glucose/cholesterol sensing. The 12-bit RC Hybrid SAR type ADC digitizes the linear sensed glucose/cholesterol value obtained from the readout circuit and sends the corresponding glucose/cholesterol digital output signal to the digital controller. A Field Programmable Gate Array (FPGA) is utilized as a digital controller platform. By using universal look up table (LUT), the digital signal is mapped into the corresponding glucose/cholesterolreadout concentration.The corresponding glucose/cholesterol readout will be displayed on the LCD and stored into the serial EEPROM.

III.CIRCUIT DESIGN AND CONSIDERATIONS

A. Dual Glucose/Cholesterol Readout Circuit

As shown in Fig. 2, to establish the low input resistance, the source terminal of MOS is chosen as input point.

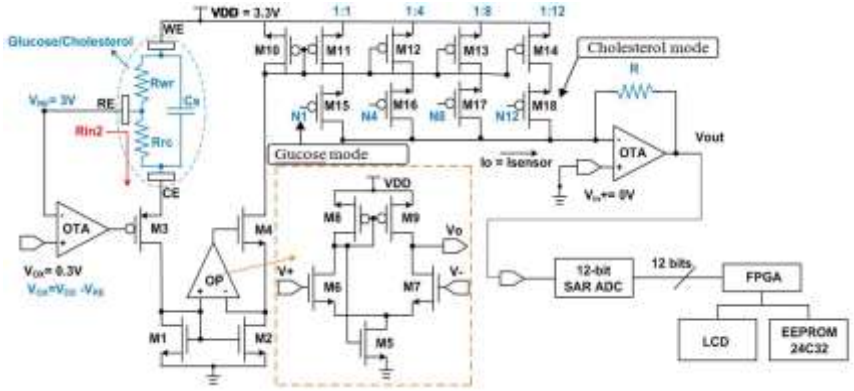

Fig. 2.Amperometric dual glucose/cholesterol readout circuit

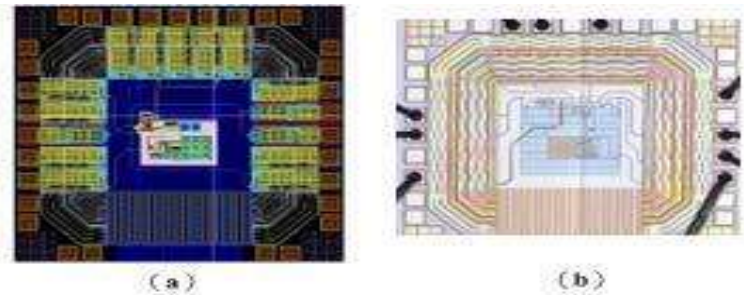

Fig. 3.Amperometric readout circuit (a) layout (b) chip fabrication

Since the readout chip test results show the best linearity of 0.997 within current range of 1μA~50μA and in order to achieve higher sensitivity of different sensing current range for glucose (5.01~22.3 μA) and cholesterol (500~600 μA), the conditioning circuit with different gain ratios is used to adjust and scale the current range into the best linearity current range. By activating transistor M15 for glucose mode or M18 for cholesterol mode, the best current range can be obtained. In addition, the transistors M1 and M2 serve as current mirror to transfer the sensor current (Isensor) into the output current (Io)[5]. As shown in Fig. 3, the readout circuit has been taped out in 0.35um TSMC CMOS technology that consumes only 409.29μW of power and occupies a small area of 0.086 mm^2.

B. Analog to Digital Converter (ADC)

In this paper, 12-bit RC Hybrid SAR type ADC will be used to complete A/D signal conversion. The principle of the proposed 12-bit RC Hybrid SAR type ADC is to implement binary approximation algorithm for converting the analog signal to digital signal. The proposed 12-bit RC Hybrid SAR type ADC consists of 5 main parts, including shift register, successive approximation register, digital to analog converter (DAC), programmable gain amplifier (PGA) as a sample-and-hold circuit (S/H) combined with the gain controller, and comparator as shown in Fig. 4.

To implement the binary search/approximation algorithm, the 12-bit register is first set to midscale (000000000000_2 to 100000000000_2, where the MSB is set to 1). This forces the DAC output (V_{DAC}) to be $V_{REF}/2$,where V_{REF} is the reference voltage provided to the 12-bit RC Hybrid SAR type ADC.

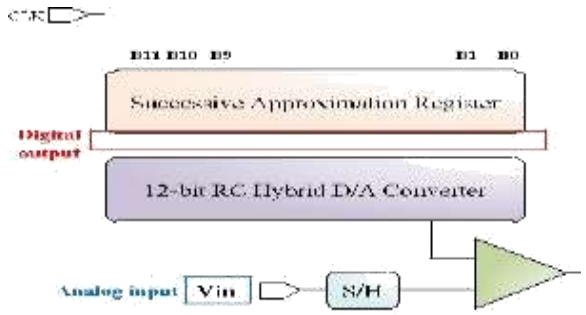

Fig. 4. Block diagram of 12-bit RC Hybrid SAR type ADC

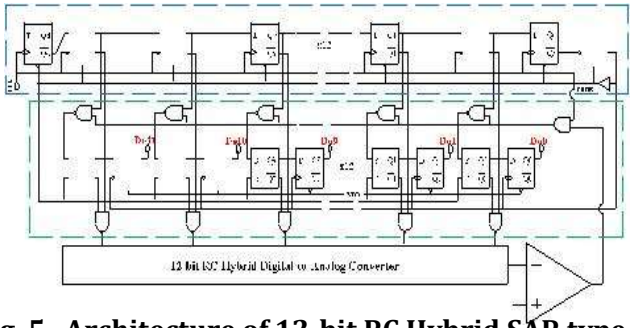

Fig. 5. Architecture of 12-bit RC Hybrid SAR type ADC

A comparison is then performed to determine if V_{IN} is less than, or greater than, V_{DAC}. If V_{IN} is greater than V_{DAC}, the comparator output is logic high, or 1, and the MSB of the 12-bit register remains at 1. On the other hand, if V_{IN} is less than V_{DAC}, the comparator output is logic low and the MSB of the register is cleared to logic 0. The SAR control logic then moves to the next bit down, forces that bit high, and does another comparison. The sequence continues all the way down to the LSB. Once this is done, the conversion is complete and the 12-bit digital word is available in the successive approximation register.

Fig. 6 shows the step simulation in which the DAC output (V_{DAC}) is approximate to the analog input with various step heights (step function). Table I shows the step simulation of ADC output (D11 to D0) from 0.0224V to 1.7646V.

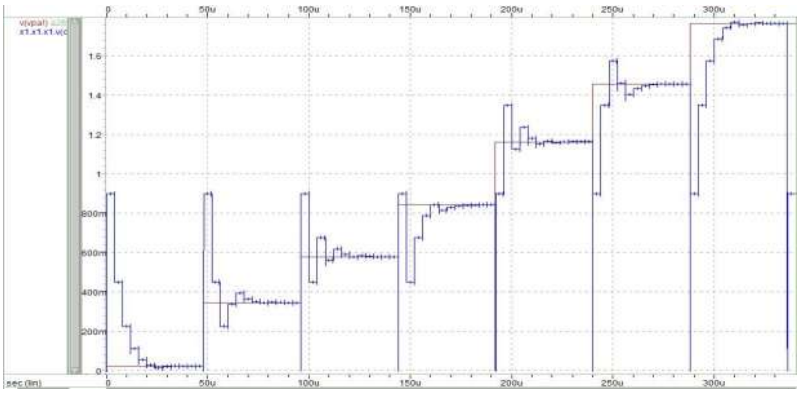

Fig. 6. Step simulation of 12-bit RC Hybrid SAR type ADC

TABLE I. STEP SIMULATION DATA EXTRACTION

Analog Input	0.0224	0.3456	0.5782	0.8428	1.1635	1.4581	1.7646
Digital Output	51	786	1316	1918	2648	3319	4015
Error	-0.27u	+0.09m	+0.3m	+0.1m	+0.17m	-0.1m	0

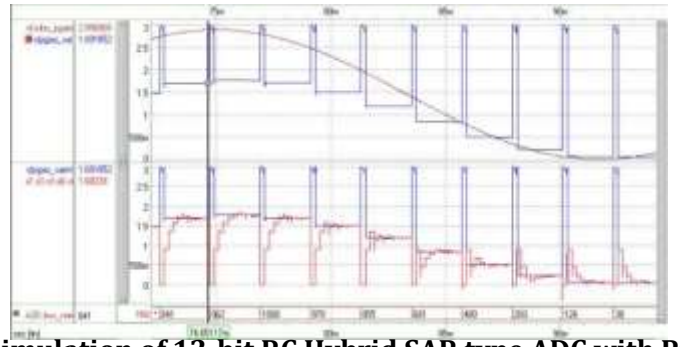

Fig. 7. Step simulation of 12-bit RC Hybrid SAR type ADC with PGA

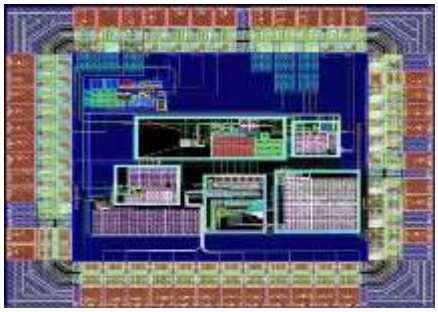

Fig. 8. Readout and 12-bit SAR ADC circuits as a front-end chip layout

As shown in Fig. 7, the front-end chip including readout and 12-bit RC Hybrid SAR type ADC circuits were fabricated (taped out) in TSMC 0.18-μm 1P6M 3.3/1.8V CMOS that consumes only 24.6528mW of power and occupies a small area of 1.4019 mm^2.

C. Altera DE2-115 FPGA

Fig. 1 shows the block diagram of dual glucose/cholesterol sensing system, in which the FPGA is used as a platform for processing the digital signal from ADC in order to be displayed on LCD and stored into serial EEPROM (24C32).

The FPGA platform consists of 12-bit to 12-bit lookup table (LUT), LCD and serial EEPROM driver modules. Since the readout circuit provides the linear output characteristic, the LUT will convert the glucose/cholesterol readout value (x) into a glucose/cholesterol concentration solution value (y)accordingly through the linear equation y = m(x) + b.

IV. MEASUREMENT SYSTEM STRUCTURE

$$v_{OUT} = \frac{N_{ADC}}{4095} \cdot 1.8\text{V} \quad (1)$$

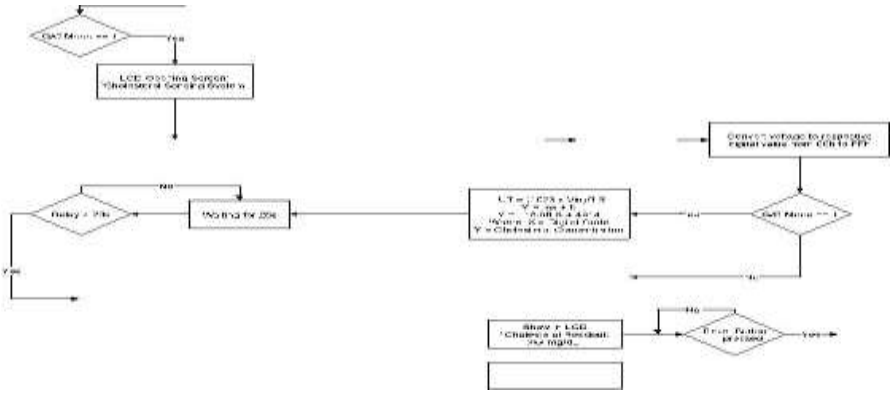

Fig. 9. Testing flowchart of the glucose/cholesterol sensing system

After waiting for 20 seconds, the LCD will show a message that the testing has been completed. Once the conversion value result is ready, the value will be written into a serial EEPROM at the same time. Finally, the LCD will display the cholesterol readout value. But once the reset button is pressed, the dual glucose/cholesterol sensing system will go back to the initial condition.

V. EXPERIMENTAL RESULT AND DISCUSSION

The verification and measurement of this system are based onFPGA platformwith the readout and ADC device. The golden results were obtained by using an electrochemical analyzer connected to personal computer with the National Instrument (NI) software.Linearity is the amount of deviationfrom aninstrument'sideal straight-line performance.The corresponding time with the best linearity is around 0.9900, which is similarto the golden results.The experiment result has been performed for glucose solution due to the wide current gap range sensitivity between 5.01~22.3 μA for glucose measurement and 500~600 μA for cholesterol measurement.The glucose measurement result is linear within a glucose concentration from 50 mg/dL to 400 mg/dL with linearity of 0.9850. The results show that the propose system works properly. As shown in Table II,compared with the other designs, this paper demonstrates several advantages, including glucose detection linearity, accuracy, and measurement time of this paper as well as the previous works [1], [2]

TABLE II. COMPARISON OF THIS PAPER WITH THE PREVIOUS WORKS

The differences	MCU [1]	PC [2]	This paper
Control unit	ATMEGA 16L	PC & NI DAQ Card	Altera DE2-115 FPGA
Controller type	Micro controller based	Micro controller based	ASIC based
Frequency	16 MHz	N/A	50 MHz
Linearity & Accuracy	0.9715	0.9715	0.985
Glucose Measurement time	15 seconds	15 seconds	11 seconds

The results in Table II show that the linearity, accuracy and measurement time of this paper are much better than other previous system designs which are using a microcontroller unit (MCU) and PC with NI DAQ[1], [2].

Since in the future, the whole system will be fabricated as a mixed signal chip by combining the digital ASICcontroller unit with the front-end circuit, it is a good approach to use FPGA as a platform for rapid prototyping purposes, simplifying the complex processing structure in a general purpose microcontroller base. By using a synchronous finite state machine (FSM) and look up table (LUT) structures for data processing, it can replace the complex structure in the general purpose microcontroller.

VI. CONCLUSIONS

A dual glucose/cholesterol sensing system was proposed. The readout circuit has been fabricated in 0.35μm TSMC CMOS technology which can operate in a current range of 1 μA to 50 μA with the linearity of 0.9971 and a power consumption of 409.29 μW with an area of 0.086 mm^2. By combining the readout circuit, 12-bit RC Hybrid SAR type ADC, LCD, and serial EEPROM with the FPGA as a platform, the dual glucose/cholesterol sensing system shows the linearity of this work is 0.9850 for the current sensing range of 5.01~22.3 μA within glucose concentration range of 50~400 mg/dL with the power consumption of this system is 46.893 mW and current sensing range of 500~600 μA within cholesterol concentration range of 150~300 mg/dL.

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