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ISSN (Online): 2455-7838

SJIF Impact Factor (2015): 3.476

EPRA International Journal of

# Research & Development (IJRD)

Volume:1, Issue:3, May 2016



Published By :  
EPRA Journals

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## REVIEW ON DMC ENCODING OF DATA FOR ENHANCED MEMORY RELIABILITY AGAINST MULTIPLE CELL UPSETS

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### ABSTRACT

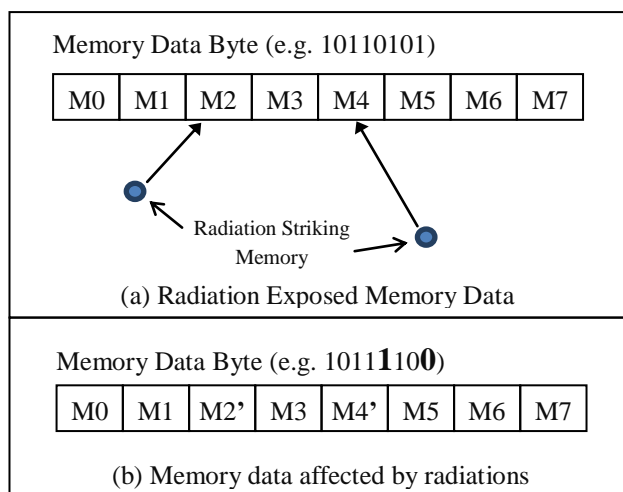
Transient multiple cells upsets (MCUs) is an important issue if consideration is the reliability of memories exposed to radiation environment. Many superior packaging technique are available which protect the memory data from radiations and transients. However, a particular packaging provides protection from a limited variation of radiations. Due to the increasing demand in the application in wireless communication field the devices are exposed to a very wide range of environment radiations. Consequently some supplementary data protection techniques are always preferred for authenticating the data before it is processed. A number of these techniques use encoded data to be stored in memories. Error correction codes (ECCs) are used to encode the data which is used to be stored in the memory. A less number of redundant bits to be stored and a minimized delay overhead in data correction are always chosen to implement an error correction code. This paper presents a review on memory data error detection and correction code.

**INDEX TERMS:** Decimal Addition, Error Correction Codes (ECCs), Error Syndrome, Hardware Memory, Multiple Cell Upsets (MCUs).

### I. INTRODUCTION

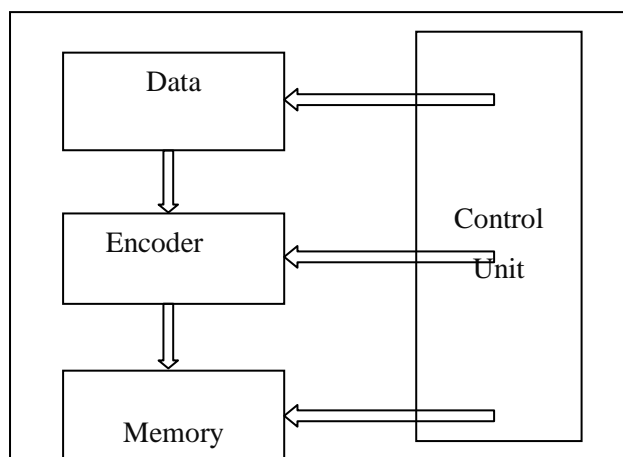
The increasing size of embedded memories electronic systems and scaling down of CMOS technology to deep nanoscale that are exposed to space environment radiations are the cause for rapidly increasing the soft error rate in memory cells. The soft error in the memories are introduced due to the radiations that have ionizing character that affect the charge stored as data in semiconductor memory. With the help of memory block the

phenomena of error generation due to radiation effect the memories that are exposed to the environmental radiations are shown by fig. 1. As shown in figure that Memory Data Byte (eg, 10110101) is to be send which is shown by M0 - M7 when this memory data is exposed to the Radiation memory data is being affected by the radiation and the send bits gets changed to e.g. (10111100).



**Fig 1. Soft Error induced in Semiconductor Memory when exposed to Energy Radiation**

While a major concern about memory consistency is single-bit error but in some cases “multiple-bit error” or “multiple cell upset” (MCUs) becomes a serious reliability concern. Many researchers recommend some error correction codes (ECCs) in order to tolerant the faults in the memory upto the maximum possible extent. A simple block diagram of the fault tolerant memory encoder implementation is shown in fig. 2.



**Fig 2. A simple data encoder block diagram**

With the help of the encoder circuit the data to be stored is first encoded to generate redundant bits for fault tolerant memories. The data and the redundant bits are stores in the memory with the help of memory interface. Decoder can use these redundant bits for correcting the errors from the memory data. only some of the most reliable codes include Bose-Choudhary-Hocquenghem (BCH) code, Reed-Solomon (RS) code and Punctured Difference Set (PDS) code. These codes have been used to deal with MCUs in memories. To control MCUs Interleaving

technique has also been used that rearranges cells in the physical arrangement to separate the bits into different physical words from the same logical word. Interleaving with content-addressable memory (CAM) is not practically used with the fixed coupling hardware architecture from both cells and comparison circuit structure. Against MCUs the researchers also proposed a single error correction and double error detection technique like Built-in-Current-Sensors (BICS). MCUs per word can be efficiently corrected by recently proposed 2-D matrix code (MC). In 2-D matrix code one word is divided into multiple rows and multiple columns, and two codes were use to protect the bits per rows and per columns and these are Hamming code and Parity code where the bits per row are protected by Hamming Code and the bits per column are protected by parity code. Two bit error detected by Hamming code is corrected by using the vertical syndrome bits. The 2-D MC is accomplished of correcting only two errors in all cases. As compared to other codes this code has a lower delay overhead.

In this paper a novel decimal matrix code (DMC) is proposed. The function of the proposed code is based on divide-symbol to provide improved memory consistency. Decimal integer addition (decimal algorithm) on the divided symbols of binary code is utilizes by the proposed DMC. To detect and correct error bits a logic comparator is used by the decoder in the proposed work to find the error syndrome. The reliability of the error detection capability of the code is enhanced by the decimal algorithm. The rest of this paper is arranged as follows: section-II presents the work published by some recent scholars under the title ‘Literature Review’. Section III presents the conclusion based on the literature review. Future scope to work using the DMC algorithm is discussed in section-IV. Finally the references are listed at the end of the paper.

**II. LITERATURE REVIEW**

In reference [1] novel per-word DMC was proposed to pledge the reliability of memory. The proposed security code utilized decimal algorithm to detect errors, so that more errors were detected and corrected. The obtained results showed that the proposed scheme has a superior protection level against large MCUs in memory. Moreover, the proposed decimal error detection technique is an striking opinion to detect MCUs in CAM because it can be combined with BICS to provide an adequate level of immunity. In reference [2] presents the comparative study of various error correcting codes which defines various alternates to overcome reliability issue of memories, when exposed to radiation. To prevent the occurrence of MCUs several error correction codes (ECCs) are used, however the main problem is that they require complex encoder and decoder architecture and higher delay overheads. The decimal matrix code (DMC) minimizes the area and delay overheads compared to the existing codes such as hamming, matrix codes, built in current sensor etc, and also improves the memory reliability by enhancing the error correction capability. In reference [3] proposed a decimal correction code for the implementation for error correction technique In order to maintain a good level of reliability, it is necessary to protect memory cells using

protection codes various error detection and correction methods are being used. Matrix codes (MCs) based on hamming codes have been proposed for storage protection. Moreover, the encoder-reuse technique (ERT) is advised to minimize the area overhead of extra circuits without interrupting the whole encoding and decoding operations. Reference [4] proposed the 64-bit decimal matrix code for detection and correction of errors in memories. To avoid MCUs from causing data corruption, more complex error correction codes (ECCs) are widely used to protect memory, but the Main problem is that they would require higher delay overhead. Newly, matrix codes (MCs) based on hamming codes have been proposed for memory protection. In proposed system increased error detection and correction rate compared to 32-bit decimal matrix code.

In reference [5] the proposed mechanism which derived from the existing codes, single error correction-double error detection-triple-adjacent error detection using hamming code and single error correction-double error detection -double adjacent error correction Codes Derived From Orthogonal Latin Square Codes will provide single and double adjacent error correction and double nonadjacent and triple error detection. These all combination is not provided any other codes. And this combined code provides correction up to double adjacent errors. In Reference [6] novel DMC was proposed to assure the reliability of memory. The proposed protection code utilized decimal algorithm to detect the errors, so that more errors were detected and corrected. The obtained results showed that the proposed scheme has a better of the protection level against large MCUs in memory. Besides, the proposed decimal error detection technique is an attractive the opinion to detect MCUs in CAM because it can be combined with the BICS to provide an adequate level of immunity. Reference [7] deals with two Error Correction Codes such as Decimal Matrix Code (DMC) and Parity Matrix Code (PMC). The DMC utilized decimal algorithm to obtain the maximum error detection capability. Moreover, the Encoder-Reuse Technique (ERT) is utilized to minimize the area overhead of extra circuits without disturbing the whole encoding and decoding processes. ERT uses DMC encoder itself to be part of the decoder. PMC utilized hamming algorithm to detect errors, so that more errors can be detected and corrected. Encoder-Reuse Technique (ERT) is also utilized in PMC to minimize the area overhead of extra circuits. The number of redundant bits is also less in PMC scheme.

In reference [8] to provide fault-tolerant memory cells, Error Correction Codes (ECCs) are used. But these codes require more area, power and higher delay overhead. Thus Matrix Codes (MCs) based on Hamming codes and parity codes are used for detection and correction of multiple errors with less decoding delay. The use of matrix codes is capable of correcting only two errors. Hence to maximize the capability of error detection and correction, Decimal Matrix Code (DMC) based on decimal algorithm is used. This algorithm utilizes decimal integer addition and decimal integer subtraction to detect and correct errors. DMC uses encoder reuse technique for fault tolerant memory protection. The use of this algorithm enables more errors to be detected and corrected by the utilization of

large number of redundant bits. Thus the framework can be modified so as to reduce the number of redundant bits by means of using parity matrix codes in which a 32 bit data is divided into 2bits of 16 blocks. Coding can be done by means of VHDL language. In reference [9] the proposed protection code utilized decimal algorithm to detect errors, so that more errors were detected and corrected. The obtained results showed that the proposed scheme has a superior protection level against large MCUs in memory. moreover, the proposed decimal error detection technique is an attractive opinion. Here the maintenance of reliability has achieved by changing Carry Save Adder (CSA). The proposed technique can also be combined with traditional 2-D repair approaches such that row and column failures and defects on multiple bits are repaired, and isolated defects are handled by the SEC-DED codes. This approach would provide a complete approach to protect against defects and soft errors in memories. Then a technique has been proposed that can deal with both types of errors effectively by applying a modified error correction process. However, for small defect rates and low failure probabilities during device operation, the probability of undetected failures will be negligible. Reference [10] proposed a hybrid matrix code for enhanced memory reliability against multiple cell upsets. For error detection and correction, for memory application with reduced area utilization and delay over heads proposed work focuses on the design of HMC. For protection it required less number of redundant bits less number of redundant bits as compared to the existing approaches. The proposed scheme showed the result obtain have a better-quality protection level against large MCUs in memory.

In Reference [11] DMC was proposed to assure the reliability of the memory. In the proposed scheme decimal algorithm is used to detect and correct the errors. So that more errors were detected and corrected. The proposed scheme showed that it has a superior protection level against large MCUs in memory and it is concluded from the obtained results. Here the only drawback is that more redundant bits are required to maintain higher reliability of memory, so that a reasonable combination of  $k$  and  $m$  should be chosen to maximize memory reliability and minimize the number of redundant bits based on radiation experiments in actual implementation. In reference [12] encoder reuse technique with DMC is proposed to correct or detect the error due to which the soft error rate in storage cell is rapidly increased. The proposed technique use decimal Algorithm based Matrix Code (DMC) uses decimal algorithm to obtain the error detection and correction capability. The Encoder-reuse technique (ERT) based DMC is use to minimize the area. Primarily, the data bits are split into symbols and they are set in a 2D matrix. The Horizontal Redundant Bits (HRB) and Vertical Redundant Bits (VRB) are computed by decimal operations in DMC encoder. After encoding, the obtained codeword is stored in the memory. If the radiation affects the memory, Multiple Cell Upset problem will happen. These troubles can be rectified in the decoder. Lastly the papers result shows that the ECC based DMC yields better performance compared to Hamming Code.

Reference [13] proposed decimal code matrix to prevent the memories from the MCUs. In the proposed method

implementation of the 32 bit Decimal Matrix code for detection and correction of errors in the memories and maintaining memory reliability are used. The proposed DMC increase the error detection and correction capability, decrease the area, power, maintain the memory reliability, and redundant bits will be reduced. Reference [14] proposed protection code DMC utilized decimal algorithm to detect errors, so that more errors were detected and corrected. The proposed method enhances the error correction capability up to 5 bits. The obtained results showed that the proposed scheme has a superior protection level against large MCUs in memory. Reference [15] proposed Decimal Matrix Code algorithm that perform decimal addition/subtraction and ex-or operation to detect and correct errors present in the memory. The decimal matrix code consumes less power than the other existing codes. The only drawback of DMC is the more number of redundant bits, which will increase the bandwidth utilization. The reduction in the number of redundant bit will in turn affect the reliability of the memory. So the redundant bits must be reduced such that it will not affect the reliability of the memory. In the proposed work parity matrix code is used to overcome the above drawback of the decimal matrix code. The parity matrix code reduces the number redundant bits. Reference [16] proposed HMC (Hybrid Matrix Code) to guarantee the reliability of the memory. Proposed method use decimal algorithm to detect or correct the error. The main downside of proposed HMC is which more number of redundant bits is obliged to keep up higher reliability. In reference [17] for providing Enhanced protection to memory a detection of multiple MCUs is an important issue which would be over come with the help of encoder reused technique by DMC. In the existing system, novel decimal matrix code (DMC) based on divide-symbol is presented which utilizes decimal algorithm to obtain the maximum error detection capability. Reference [18] proposed decimal matrix code which provides an efficient error correction code in which the reliability and security of the memory is improved. The proposed code uses decimal algorithm which possess integer addition and subtraction which is simpler than the binary algorithm which performs bit wise logical operation. The binary algorithm uses only limited number of syndrome bit whereas the decimal matrix code uses more syndrome bit namely 20 horizontal syndrome bit and 16 vertical syndrome bit respectively which constitute a total of 36 bit. A single encoder is used in the DMC architecture that act as encoder as well as syndrome calculator, this will reduce the area overhead. The decimal matrix code consumes less power than the other existing codes.

### III. CONCLUSION

To assure reliability and a 32-bit word is encoded and decoded with the help of proposed DMC in presence of MCUs with reduced performance overheads. With the help of the encoder circuit the whole circuit area of DMC can be minimized. This shows how the area overhead of extra circuits can be substantially reduced.

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