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LOW POWER FULL SWING XOR AND XNOR STRUCTURES FOR FULL ADDER CIRCUITS

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ABSTRACT

As the scale of integration increases, the usability of circuits is restricted by the more amounts of power and area consumption. The growing popularity demands for battery operated devices such as mobile phones, tablets and laptops. By reducing the number of transistors in the conventional circuits we have proposed two full adder circuits which is having advantage of consuming low power when compared to the other two conventional circuits. In this project XOR-XNOR gates are used to implement full adder structures. These circuits are going to be optimized in terms of power consumption and delay, which are due to low output capacitance adder. One-bit full adder circuit is proposed based on novel full-swing XOR-XNOR gates. To investigate the performance of the circuits Tanner Tools and HSPICE are used. This simulation is based on 90nm technology. The simulations result in high and speed and low power against other full adder designs. These circuits are to be simulated in the terms of variation of the supply, output capacitance and the size of transistors. These circuits have their own merits in terms of speed, power consumption, power delay product and driving ability

***INDEX TERMS*: Capacitance adder, Delay, Low power.**

I. INTRODUCTION

Today the electronic systems are a part of everyday life. Increased usage of operated portable devices, like cellular phones, personal digital assistants (PDAs) demand VLSI and ultra-scale large integration designs with an improved power delay Characteristics. The efficiency of many digital applications depends on performance of arithmetic circuits such as adders, multipliers, comparators and dividers. Full adders act as a core component of the complex circuits for multiplication and division and thereby influence the overall performance of the entire system. Full adder is a basic building block or component used in architectures of VLSI. Adder circuits are used in arithmetic logic circuit designs, processor chip like Snapdragon, Exynos, or Intel Pentium for CPU part.

In VLSI, the trade-off factors are low power consumption, delay, speed, cost. Several logic styles full adders [1]. Every circuit has its own advantages and disadvantages based on power and delay

The rest of the paper is organized as follows. In Section II the circuits for XOR-XNOR gates, Section III proposed circuits of XOR-XNOR gates and six new full adders are designed, Section IV consists of newly proposed Full adders Section V have the simulation results of the proposed circuits and Section V concludes the paper.

II. REVIEW OF XOR AND XNOR GATES

Figure 1 shows the Full Swing XOR/XNOR circuit designed by using Double pass – transistor logic (DPL) style [1]. This structure has 8 transistors. The main disadvantage of this circuit is using 2 NOT gates which consumes high power because NOT gates must drive output capacitance. Therefore, size of transistors in NOT gates should be increased to obtain lower delay with large capacitance it causes the creation of intermediate node. Therefore, power dissipation and short circuit power are increased, delay will also increase.

Figure 2 shows the Full Swing XOR/XNOR circuit designed by using Pass – transistor logic (PTL)[1] style. This structure has 6 transistors. This circuit has less delay and power consumption which are better than Figure 1. Here XOR circuit has lower delay than its XNOR circuit. The only problem in this circuit is using NOT gates in critical path. Delay is low in XNOR circuit because critical path of XOR circuit is composed of a NOT gate with NMOS transistor. But critical path of XNOR circuit is comprised of NOT gate and PMOS transistor which is slower than NMOS. Therefore, to

improve the XNOR circuit speed, the size of PMOS transistor and NOT gates should be increased.

Figure 3 shows the XOR/XNOR circuit designed by using complementary pass – transistor (CPL) style [1][6]. The problem in this circuit is XOR/XNOR circuit should have feedback on outputs which increases delay [3] and short circuit power of the structure. To overcome the delay size of transistors is increased. Another disadvantage is having 2 NOT gates in critical path. If we remove two transistors (a NOT gate) then it will reduce the power dissipation in the circuit

The non -full swing circuit is efficient in terms of power and delay. But disadvantage is the voltage drop in the input values. To solve this problem XOR and XNOR structures are implemented. For all inputs the output has full swing there will be no NOT gates in XOR and XNOR circuits. Even there is an extra transistor in the XOR and XNOR gates when compared to non-full swing circuits, there is an advantage of l good driving capability, high speed and low dissipation.

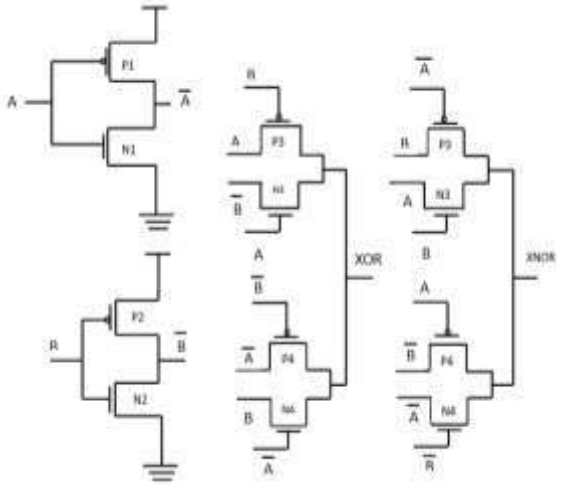

Fig. 1: Full Swing XOR/XNOR gate using double pass

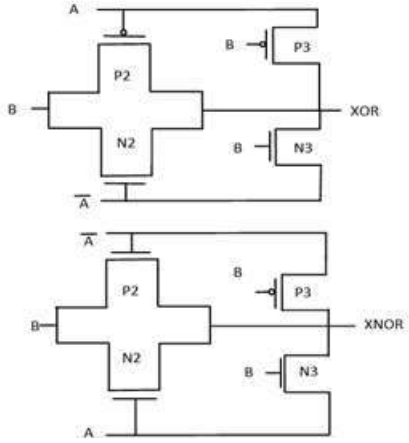

Fig. 2: Full Swing XOR/XNOR gate using PTL

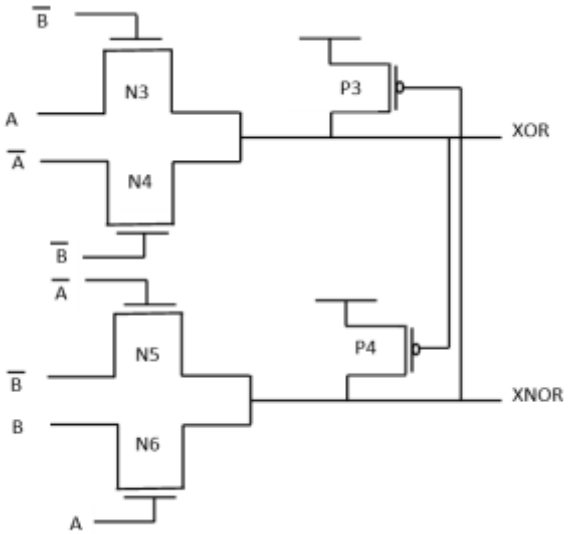

Fig. 3: Full Swing XOR/XNOR gate using CPL

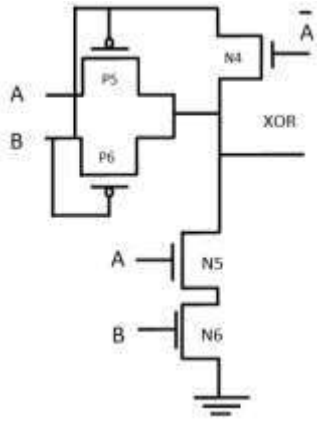

Fig. 4: Full Swing XOR gate

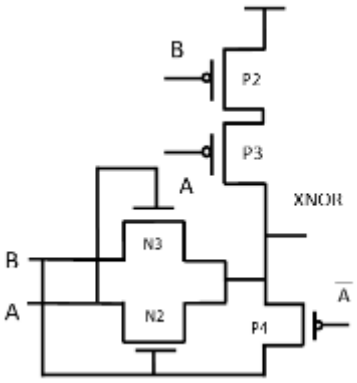

Fig. 5: Full Swing XNOR gate

III. DIFFERENTIAL FULL ADDER STRUCTURES

Figure 6 show the first Full Adder circuit (20T – Full Adder) which is made up of 2 to 1 Mux gates and XOR and XNOR gate. This circuit has high power consumption NOT gates on critical path and consists of 20 transistors. Advantage is full swing output, low power dissipation, high speed and robustness against supply voltage scaling, transistor sizing [7]. Disadvantage is reduction of output driving capability when it is used in chain structure such as ripple adder.

Figure 7 shows the second Full Adder circuit (17T - Full Adder). This 17T – Full Adder is designed by using the XOR gate. This is made up of 17 transistors that have less than the Figure 4 circuit. Delay of 17T – Full Adder is higher than that of 20T – Full Adder due to addition of NOT gates on critical path of17T – Full Adder. Power consumption of 17T – Full Adder [1] is less than that of 20T – Full Adder due to reduction in number of transistors. But the NOT gates of this circuit increases short circuit power. So the power dissipation does not reduce. The NOT gates improve the output capability circuit.

Figure 8 shows the third Full Adder circuit (26T – Full Adder Buffer). This circuit has 26 Transistors. There are XOR-XNOR gate, one 2-1 Mux gate and NOT gate on critical path [8]. It has buffers on sum and Cout outputs. Buffers are used in the output because VLSI circuits degrade due to creation of parasitic capacitors and resistors during the fabrication as well as increasing the Threshold voltage of transistors over time. The output NOT gates reduce the resistance from input of the circuit to VDD, Ground. Disadvantage is power consumption and delay is more when compared to previous adder [1].

Figure 9 shows the fourth Full Adder circuit with new buffers (26T – Full Adder New Buffer). In this circuit the buffers are placed in the place of 2 to 1 Mux gate instead of placing them at output. This circuit consists of 26 transistors. Three additional NOT gates are required. Thus circuit consists of an XOR and XNOR gate [9] and a 2 to 1 Mux gate and delay is reduced compared with the 26T – Full Adder New Buffer. Driving capability is slightly less than that of 26T – Full Adder New Buffer due to existing 2 to 1 Mux gate between the buffer and output node[1].

Figure 10 represents the fifth Full Adder circuit (22T – Full Adder). Due to the presence of Cbar signal which produces sum, XOR and XNOR signals through multiplier but they are connected to data select lines of 2 to 1 MUX. So capacitance of XOR and XNOR modes become smaller and delay [3][5] is improved. Power consumption and delay of 22T – Full Adderis less when compared to20T – Full Adder Buffer, inspite of having two transistors more, due to less capacitance of XOR and XNOR modes. By adding Cbar signal driving capability is more than previous circuits [1].

Figure 11 represents the sixth Full Adder circuit (19T – Full Adder). Due to the presence of Cbar signal which produces sum, XOR and XNOR signals through multiplier but they are connected to data select lines of 2 to1 MUX. So capacitance of XOR and XNOR modes become smaller and delay is improved. Power consumption and delay of 19T – Full Adder is less when compared to 17T– Full Adder, inspite of having two transistors more, due to less capacitance of XOR and XNOR modes, by adding Cbar signal driving capability is more than previous circuits [1].

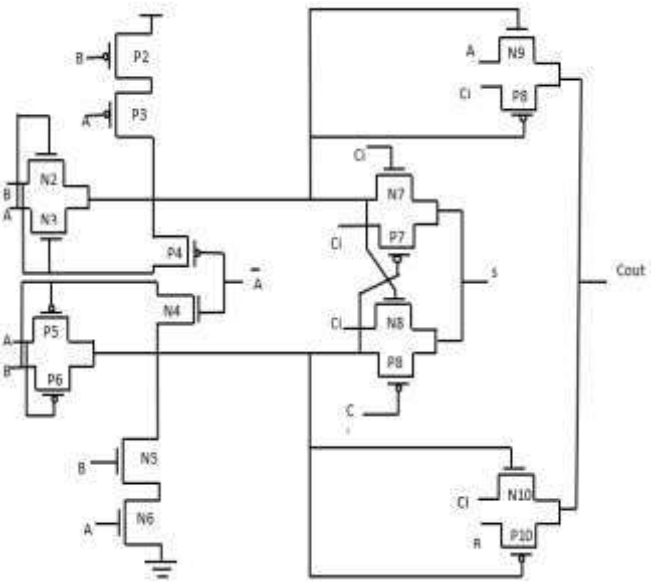

Fig. 6: 20T Full Adder

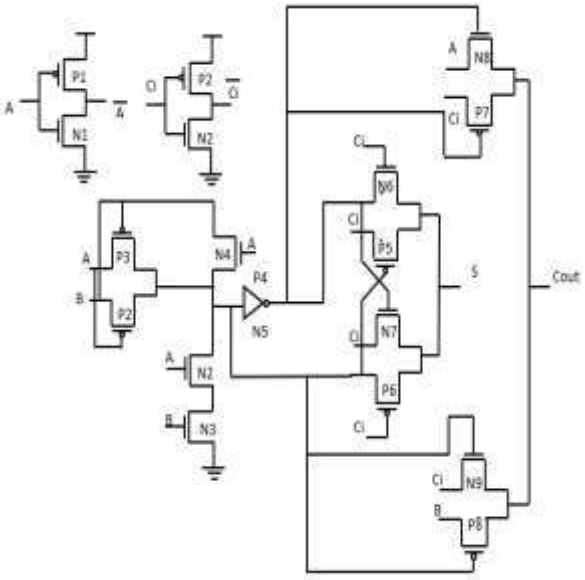

Fig. 7: 17T Full Adder

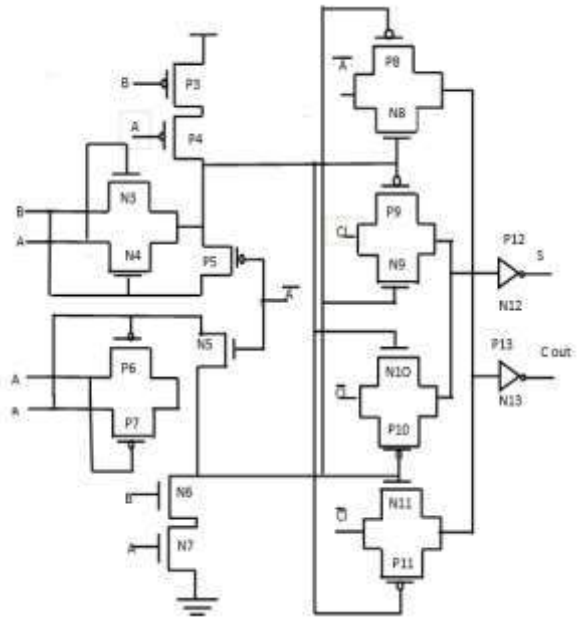

Fig. 8: 26T Full Adder Buffer

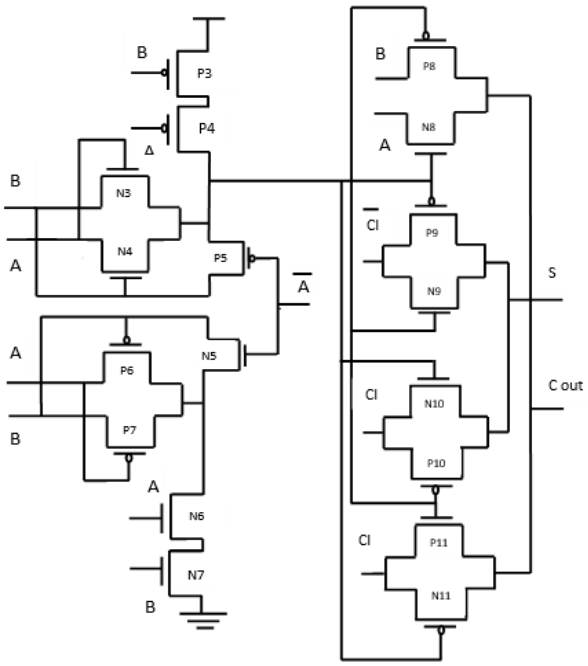

Fig. 10: 22T Full Adder

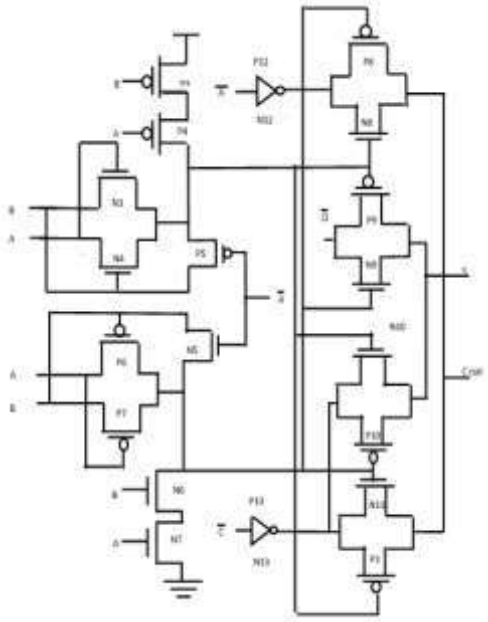

Fig. 9: 26T Full Adder New

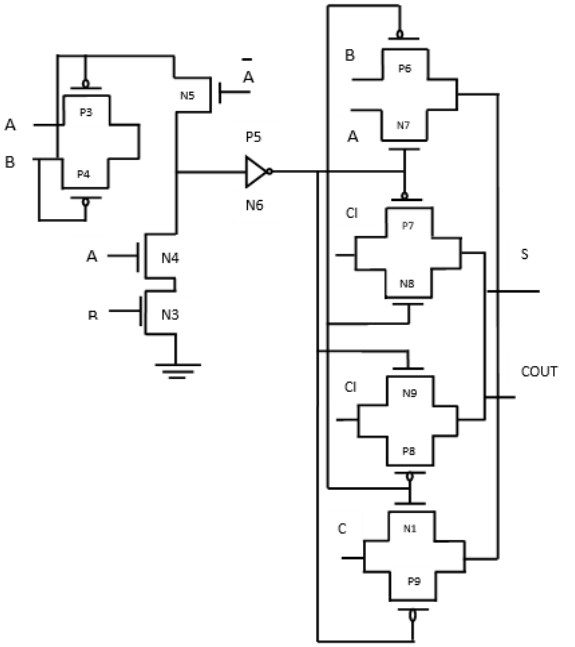

Fig. 11: 19T Full Adder

IV. PROPOSED FULL ADDER CIRCUITS

Use Figure 12 represents the first proposed Full adder. The circuit consists of 18 transistors which have two transistors less when compared to 20T – Full Adder. This circuit has less power consumption and low delay. This circuit works in non – full swing, due to this the outputs have non – full swing effect. But there is no Disadvantage in having non – full swing outputs. The proposed full adder has low power consumption when compared to the previous circuit 20T– Full Adder due to the presence of less number of transistors and occupies less space due to the removal of two transistors [1][2].

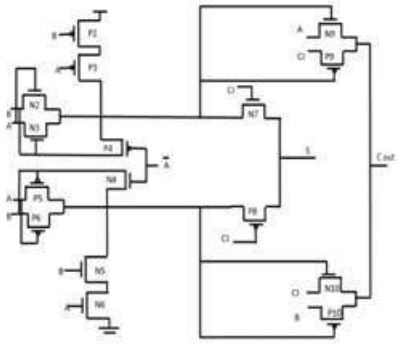

Fig. 12: Proposed Full Adder

Figure 13 represents the second proposed Full adder. The circuit consists of 15 transistors which have two transistors less when compared to 17T– Full Adder. This circuit has less power consumption and low delay. This circuit works in non – full swing, due to this the outputs have non – full swing effect. But there is no Disadvantage in having non – full swing outputs. The proposed full adder has low power consumption when compared to the previous circuit 17T – Full Adder and occupies less space due to the removal of two transistors [1][2].

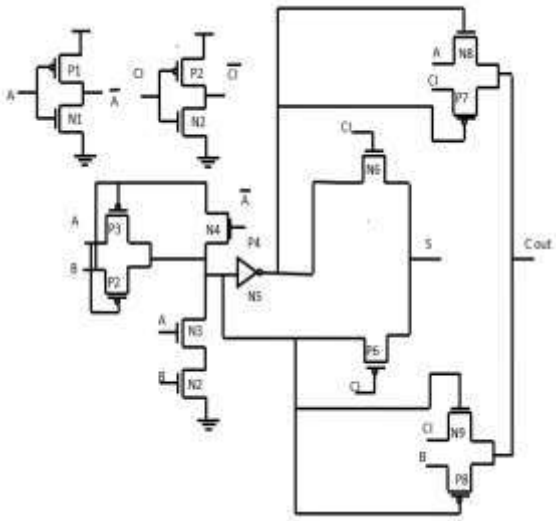

Fig. 13: Proposed Full Adder 2

A. Simulated Results and Performance Comparison

. Table 1: Full Adder Comparison table

DESIGN	POWER	DELAY (SUM)	DELAY (CARRY)
20T – Full Adder	19.97µW	6ns	10ns
17T Full Adder	21.410µW	2ns	6ns
26T – Full Adder Buffer	1.8072µW	2ns	8ns
26T – Full Adder New Buffer	1.5994µW	6ns	6ns
22T – Full Adder	19.902µW	8ns	1ns
19T – Full Adder	12.580µW	8ns	8ns
Proposed Full Adder 1	0.3216µW	2ns	6ns
Proposed Full Adder 2	0.34928µW	2ns	6ns

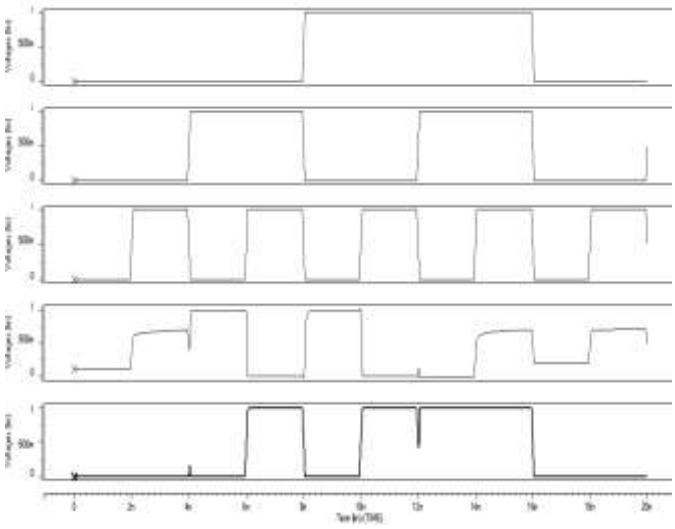

Fig. 14: Proposed Full Adder 1

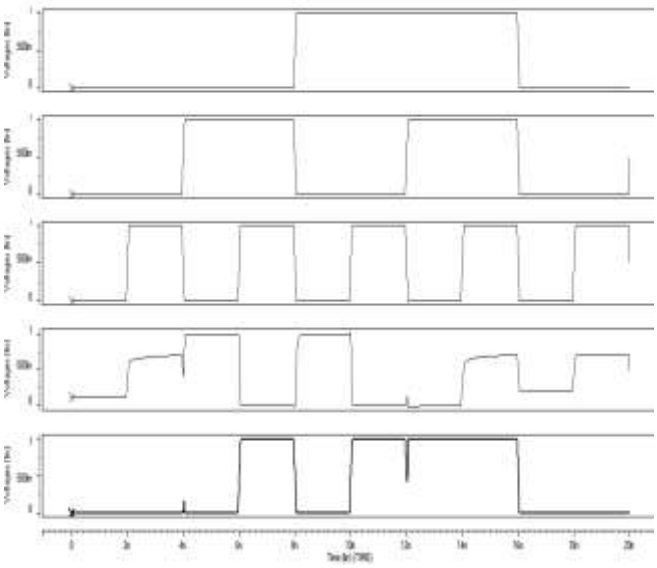

Fig. 15: Proposed Full Adder 2

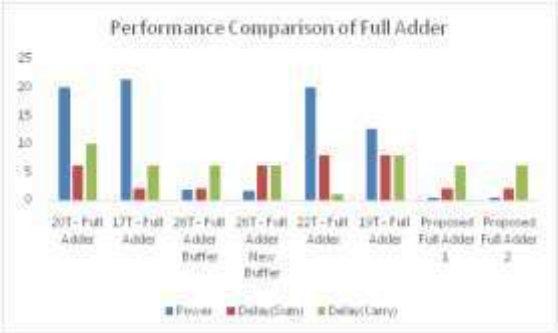

Fig. 16: Graphical Representation of Power and Delay

V. CONCLUSION

In this paper, the low power and fast full adder circuits are designed by using XOR and XNOR gates. This work presents low power consumption of a 1-bit full adder design in 90nm technology. The proposed full adder circuits occupy less space due to number of transistors which consumes less power and which is operated at high speed when compared to the convectional full adders. The proposed full adder 1 circuit is implemented by removing the P7 and N8 transistors which in turn reduces the circuit complexity. Similarly, in the proposed full adder 2 circuit is implemented by removing the P5 and N7 transistors which in turn reduces the circuit complexity. Similarly, in the proposed full adder 2 circuit is implemented by removing the P5 and N7 transistors.

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