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A NEW FIFTEEN LEVEL INVERTER TOPOLOGY WITH LESSER HARMONICS AND LESSER NUMBER OF SWITCHES

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ABSTRACT
Multilevel Inverters play a vital role in all applications of the world,particularly in industry.The industry is currently in need of adjustable speed drive, which should have lesser amount of THD.So, the usage of multilevel inverters is inevitable.Further,nowadays in solar energy systems multilevel inverters have started finding their place.But, the important restriction in multilevel inverter is the number of switches present in it.As the number of switches increase,switching loss also increases and cost increases.Research works are in progress towards this approach.In this work a novel 15 level inverter with 12 switches has been presented.Out of this ,eight switches are used for switching various levels and for switches are used to determine the polarity.Simulation of the topology has been performed in MATLAB Simulink environment.Hardware results have been also presented.In the hardware, a provision to vary the speed, by varing frequency in discscrete manner by providing selector switches were also included.The results show that the THD is within 10% value.

I.INTRODUCTION

To achieve more level of voltages with lesser number of switches in Multilevel inverters with lesser along with lesser Total Haronic Distortion has been an long time research work around the world since it has been found difficult to get pure sine wave in the output of the multilevel inverter.Nabae et al proposed first a two level inverter topology for resistive load.X,Yuan proposed a diode clamped multilevel inverter which removed the necessities of series clamping of inverters and synthesised required output voltages with lesser number of diodes[2].Marchesonni etal proposed a diode clamped multilevel inverter with DC capacitors along with a way to control DC link voltages[3].Maheshkumar and Divya proposed a new Flying capacitor multilevel inverter ogf H bridge type with relatively lesser number of switches and were able to synthesise the voltage to the required levels[4].A shukla et al proposed multilevel inverter topology and tested it for reactive power control [5].In flying capacitor multilevel inverter voltage balancing was a big problem.To address this, G.P Adam etal, proposed a new flying capacitor multilevel inverter topology by replacing capacitors with half bridge

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cells and made it flexible to estend it to any number of levels[6].The adjustable speed drives were replaced from conventional two level inverter to higher level inverters.During this transition, the harmonics in their stator was huge problem.To avoid that a new topology of induction motor itself was developed in which two ends of each winding of each of each phase of stator was left open and called as open end winding induction motor drive.K.Gopakumar et al developed a new three level inverter topology for such motor which had the advantages of eliminating triplen harmonics and balancing DC link voltages[7].P.S.Channdrasekhar et al., proposed a new topology which was hybridized nature of diode clamped and flying capacitor multi level inverters,in which they used only two capacitors to divide the voltage[8].Space vector modulation was new technique to derive switching states and hence to make appropriate method to switch the switches of inverter.Siouitra das etal,derived certain mathematical expressions for harmonic distortion factors[8].Roshankumar et al formulated three phase H bridge inverter by cascading three single phase H Bridge inverter and tested the capacitor balancing for sudden acceleration of the motor and shown very good capacitor balancing methodology[10].Capacitor voltage balancing was done by predictive control method by using a cost function and lesser value of the cost function yielded better switching angle[11].M.Sandhya et al proposed a novel fifteen level inverter which had lesser THD[12].But their work had several DC sources.So, in this work they are replaced with one DC source and same output voltage is obtained by dividing the voltage by using 8 number of same valued capacitors.

II.PROPOSED TOPOLGY

Large number of sources in an inverter increases its cost.Further,if the value of voltage sources change due to their chemical composition,it will create problems in the output of the inverter.So, in this work large number of sources in [12] has been replaced by a single source.This voltage is divided equally by capacitors and available to each switch.Such a topology is shown in fig.1.

It has eight switches,numbered from S1 to S8.Each switch is subjected at the ost to a voltage of V/8. Switches SP1 to SP4 are polarity determining switches.SP1 and SP3 are useful for producing positive polarity and for producing negative polarity,SP2 and SP4 are to be switched.In this anner the same 15 level voltage can be synthesised at the output of inverter with a single source. As number of switches is less it experiences lesser switching loss.In addition the total harmonic distortion has been reduced considerably.

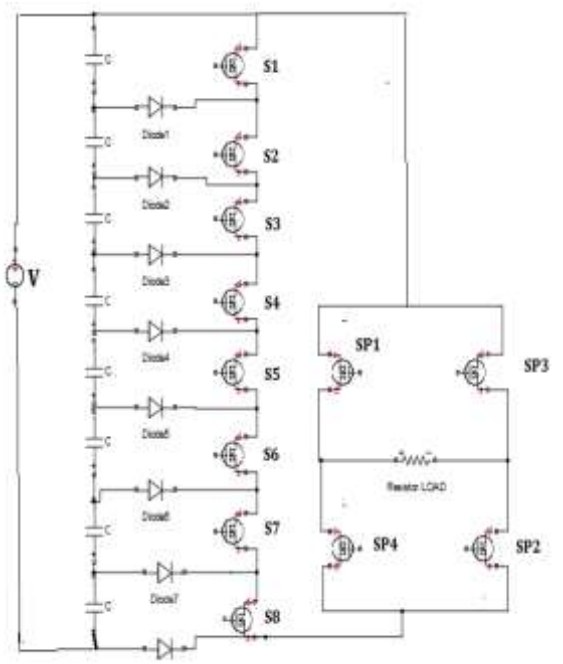

Fig.1.Proposed Inverter Topology

In the above said inverter DC source is realised by Recifier followed by filter This capacitor filter has lesser ripples.So the DC Voltage is easily obtained from AC source in a easier manner.The block diagram of the system is shown in fig.2,

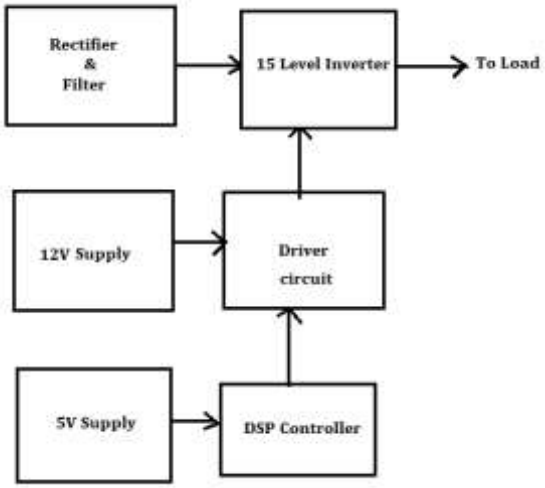

Fig2.,Block diagram of the proposed system

The levels of inverter is realised by switching the level switches S1 to S8.To realise voltage of V/8 the switch S1 alone is turned on. To realise V/4 S1,S2 are to be turned on. Similarly

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for realising 3V/8,switches S1,S2 and S3 are to be turned on.All switches are turned on to realise the full voltage of V.

Next important aspect is polarity of the voltage.To realise voltage of +V/8,along with S1, switches SP1 and SP2 are to be turned on.For the same case of -V/8, apart from S1, switches SP3 and SP4 are turned on.Similarly, for synthesising V/4, apart from S1 and S2,SP1 and SP2 are turned on. Similarly for synthesising `-V/4,apart from S1 and S2, switches SP3 and SP4 are turned on.Now it is evident that for positive polarity, switches SP1 and SP2 are turned on. For negative polarity switches SP3 and SP4 are tuned on.This topology is essentially a combination of inverter and H bridge.The various voltage levels and the corresponding switches to be turned are given in the following table:

TABLE-I
Synthesisation of Voltages in The Prposed Topology

Level	Switches of Level	Switches of Polarity
+Vdc	S1,S2,S3,S4,S5,S6,S7, S8	SP1,SP3
+7Vdc/8	S1,S2,S3,S4,S5,S6,S7	
+3Vdc/4	S1,S2,S3,S4,S5, S6	
+5Vdc/8	S1,S2,S3,S4,S5	
+Vdc/2	S1,S2,S3,S4	
+3Vdc/8	S1,S2,S3	
+Vdc/4	S1,S2	
+Vdc/8	S1	
0	None	None
-Vdc/8	S1	SP2,SP4
-Vdc/4	S1,S2	
-3Vdc/8	S1,S2,S3	
-Vdc/2	S1,S2,S3,S4	
-5Vdc/8	S1,S2,S3,S4,S5	
-3Vdc/4	S1,S2,S3,S4,S5, S6	
-7Vdc/8	S1,S2,S3,S4,S5,S6,S7	
-Vdc	S1,S2,S3,S4,S5,S6,S7, S8	

It is clear that the understanding and implementation of the switching sequence of the topology is easy .So, coding in dSPIC controller is simple and capacitor voltage can also be easily be balanced.Thus, it has been proven that with 12 switches alone,15 level output voltage can be easily realised.

III.SIMULATION RESULTS

The proposed Topology was simulated using MATLAB R2014 Simulink environment.IGBT was used as switch. A small voltage of 20V was used for simulating the circuit.The simulation output along with THD analysis was performed.The simulation results are depicted below:

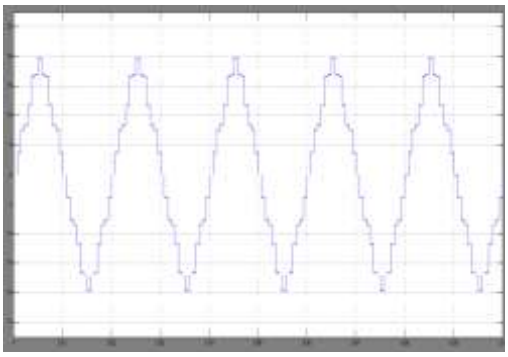

Fig.3.Fifteen Level Inverter Output voltage

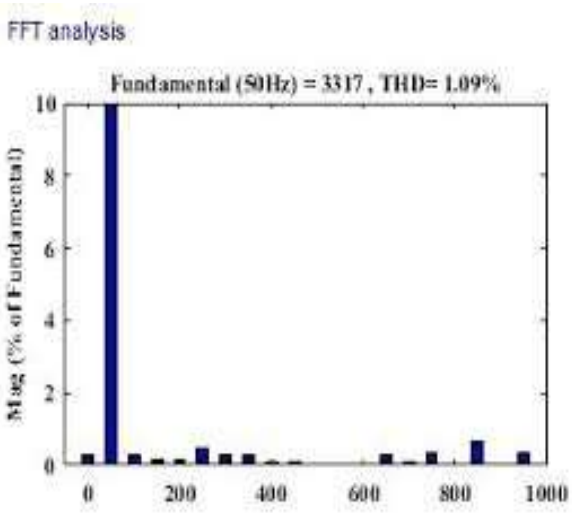

Fig.4.FFT Analysis of the Proposed system

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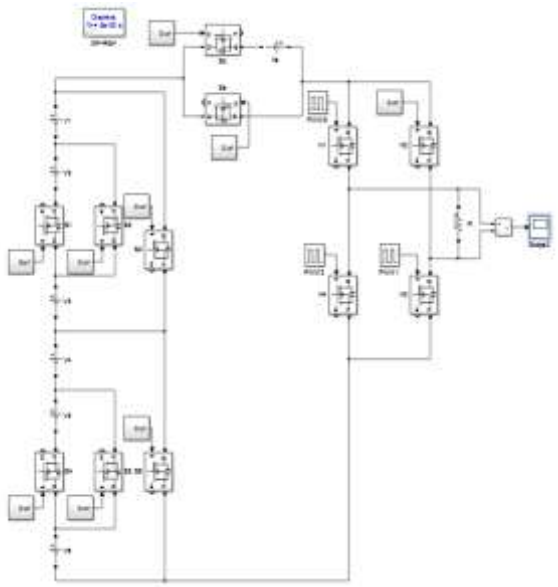

Fig.5.Simulation Circuit in MATLAB

From the above simulation it is evident that the THD is around 10%.So, lesser is the THD the greater is the applicability of topology to Induction Motor.So, this topology is better for applying on Induction motor.

IV.IMPLEMENTATION

The topology was implemented with IGBT IRGP406 with the switching pulse generated by dsPIC30F4011 and was tested for its output.The output voltage was upto the expected level .The toplogy was tested with a small 0.5HP single phase induction motor and the motor worked smoothly.

Further a selector switch was placed in the protrotype to vary the frequency and hence the speed of the motor.Three codings were given in DSP controller to select a particular code for particular frequency.The hardware and the results obtained are given below:

The results of hardware setup shows that the voltage synthesized meets the required level.Also the motor running was smooth and without noise.

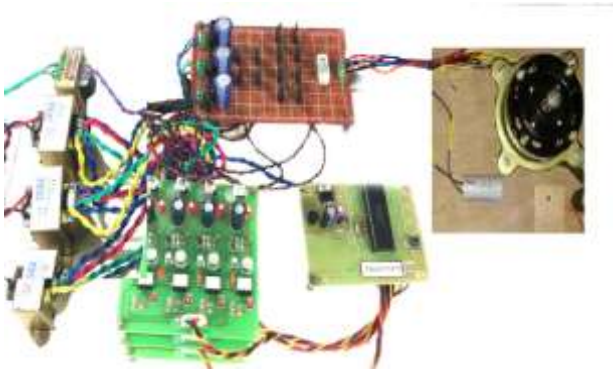

Fig.6.Experrimental Setup

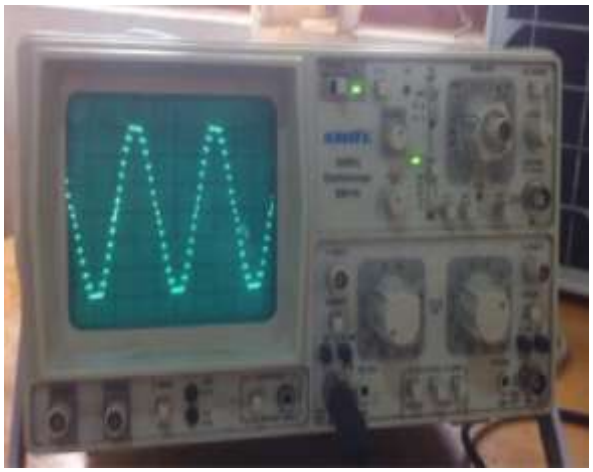

Fig.7.Output Voltage

TABLE-II
FREQUENCY VS SPEED

Selector switch	Frequency(Hz)	Speed(rpm)
1.	25	550
2.	35	980
3.	50	1440

V.CONCLUSION

Thus a novel 15 level inverter was proposed in this work.It has 8 switches for realising levels and 4 switch H Bridge for determining polarity.The topology was simulated in MATALB and the results were found satisfactory.The simulation results show that the THD level is around 10%.The hardware also was tested with IGBT as switching device and coding was done in dsPIC30F4011.The toplogy was tested with resistive load as well as induction motor.The output voltages with resistive loads were satisfactory.The speed of induction motor was varied by varying frequency levels by using selector switch.the variation in speed was satisfactory.Now the work is in progress towards the balancing the capacitor voltage.

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