ISSN (Online): 2455-7838
SJIF Impact Factor (2015): 3.476

EPRA International Journal of

Research & Development

(IJRD)

Volume:1, Issue:9,November 2016

Published By :
EPRA Journals

SJIF Impact Factor: 3.476 ISSN: 2455-7838(Online)
EPRA International Journal of Research and Development (IJRD)
Volume: 1 | Issue : 9 | November | 2016

IMPLEMENTATION OF QUANTUM CELLULAR AUTOMATA TECHNOLOGY AND COMPARISON WITH CMOS TECHNOLOGY

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ABSTRACT

In this paper, a quantum dot cellular automata Inverters, Nand, Nor gates and adder designs are presented. These designed circuits are compared with Conventional CMOS technology. QCA has been recognized as one of the technologies that may replace FET based computing device at the nanoscale level. The aggressive scaling of CMOS technology has entered a regime that any more scaling integration creates several operating and performance degrading issues. Today several layers of Interconnects over connecting 40 million transistors together and makes the routing complexity huge and hence device propagation delay dominates and occupy most space of the chip. One way to eliminate interconnection delay, switch to QCA technology. This paper discusses about QCA technology and Compared with the CMOS Circuits and it was found that QCA circuits has higher speed, less area and reduced power consumption over CMOS technology.

KEYWORDS: *CMOS technology, quantum cells, logic primitives*

1. INTRODUCTION

Quantum dots are nanostructures created from standard semi conductive materials (GaAs)[1],[2]. These structures are modeled as quantum wells. They exhibit energy effects even at distances several hundred times larger than the material system lattice constant. A dot can be visualized as well. Once electrons are trapped inside the dot, it requires higher energy for electron to escape. Quantum dot cellular automata is a Novel technology that attempts to create general computational functionality at the nanoscale by controlling the position of single electrons. The fundamental unit of QCA is QCA cell created with four quantum Dots positioned at the vertices of square. The electrons are quantum mechanical particles. They are able to tunnel between the dots in a cell. The electrons in the cell that are placed adjacent to each other will interact. As a result the polarization of one cell will be directly affected by the polarization of its neighboring cells. Fig 1 below shows quantum cells with electrons occupying opposite vertices.

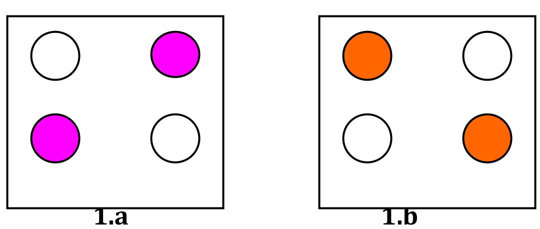

Fig 1 shows QCA cells with four quantum dots.1.a →P = +1 (Binary 1) 1.b→ P = -1 (Binary0) [1].This interaction forces affects neighboring cells to synchronize their polarization. Therefore an array of QCA cells acts as wire and is able to transmit the information from one end to another.

2. QUANTUM COMPUTATION

To perform logic computing, we require universally a complete logic set. We need a set of Boolean logic gates that can perform AND, OR, NOT and FANOUT operations. The combination of these is considered as universal because any general Boolean function can be implemented with combination of these logic primitives. The fundamental method for computing is majority gate or majority voter method by konrad walus. Suppose three inputs are given to Quantum circuit. Then output of the quantum structure is tabulated in table1. The majority gate produces an output that reflects the majority of the inputs. The majority function is a part of a larger group of functions called threshold functions. Threshold functions works according to inputs that reaches certain threshold before output is asserted

INPUT	OUTPUT MAJORITY VOTING
000	0
001	0
010	0
011	1
100	0
101	1
110	1
111	1

Table 1 – Majority voting scheme

The majority function is most fundamental logic gate in QCA circuits. In order to create an AND gate we simply fix one of the majority gate input to 0 (P = -1). To create OR gate we fix one of inputs to 1 P = +1. The inverter or NOT gate is also simple to implement using QCA. If we place two cells at 45 degrees with respect to each other such that they interact inversely.

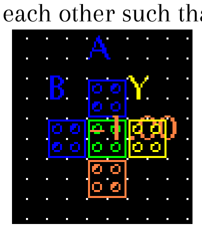

Fig 2.Majority AND gate – QCAD TOOL

The output of majority AND gate reflects the majority of the inputs. Suppose input A =1, B = 1, Control input 0(-1), the output is equal to 1.

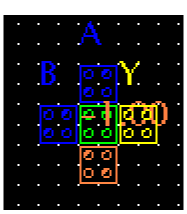

Fig 3 Majority OR gate – QCAD TOOL

Control input to OR gate is 1.

3. QCA CLOCKING

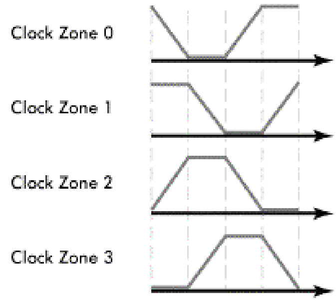

Figure 4 shows clocking scheme of QCA circuits

Clocking is the requirement for synchronization of information flow in QCA circuits. It requires a clock not only to synchronize and control information flow but clock actually provides power to run the circuit. The cells are not powered from any other external source apart from the clock. These clocks have been proposed to control the potential barriers between the quantum dots. When the clock signal is high the potential barriers between the dots are low and electrons effectively spread out in the cell and no net polarization exists. (P = 0) As the clock signal is switched low, the potential barriers between the dots are raised high and the electrons are localized such that a polarization is developed based on the interaction of their neighbors.

In short when clock is high cell is unlatched and when clock is low cell is latched. In order to pump information down a circuit in a controllable manner four clocking zones are available as shown in Figure 4. Each of clocking signal lagging in phase by 90 degrees with respect to one before. In this way, the cells are latched in series and propagate information in the same direction. So clocking is essential for quantum circuits.

4 QCA CIRCUITS AND COMPARISON WITH CMOS CIRCUITS

In this section, some of the Combinational circuits are presented using QCA designer and compared with CMOS using Micro wind tool.

4 STUDY I

4.1 QCA INVERTER

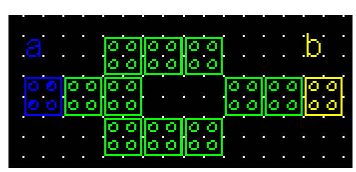

Figure 5 QCA inverter a –Input and b- output.

Figure 5 shows QCA inverter and 6 shows simulated waveform. Table II gives details about the various parameters during simulation.

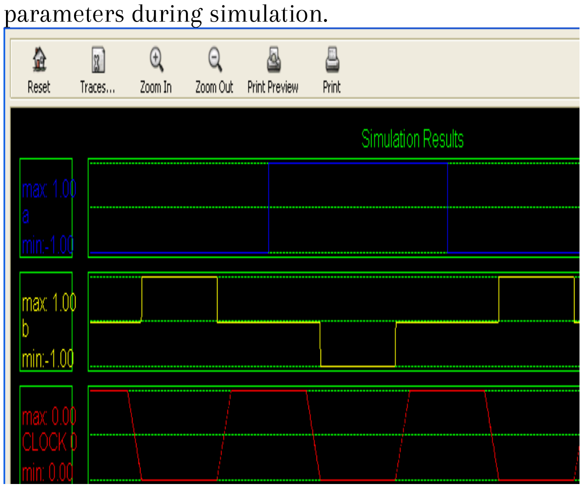

Figure 6 Simulated waveform for Inverter.

S.NO	PARAMETER	VALUE
1	SPEED	6.7 ns
2	AREA	5000 nm^2
3	TEMPERATURE	5 K
4	REL PERMITIVITY	12.9
5	RADIUS OF CELL	65 nm
6	CLK HIGH	9E -20
7	CLK LOW	3E-21
8	SIMULATION	BISTABLE / DIGITAL

Table II Inverter – Parameter Values

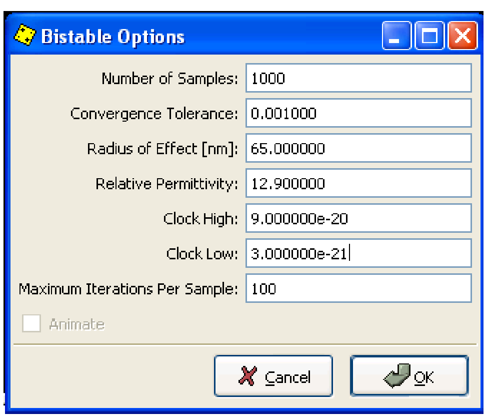

Figure 7 Parameter from QCAD

4.2 CMOS INVERTER

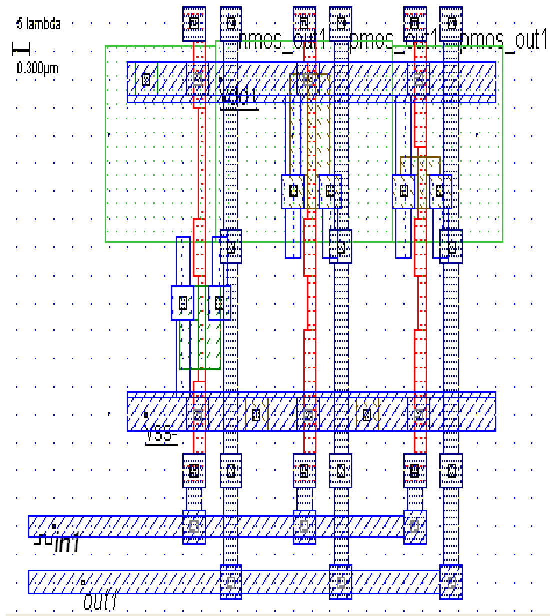

Figure 8 shows CMOS inverter from Micro wind.

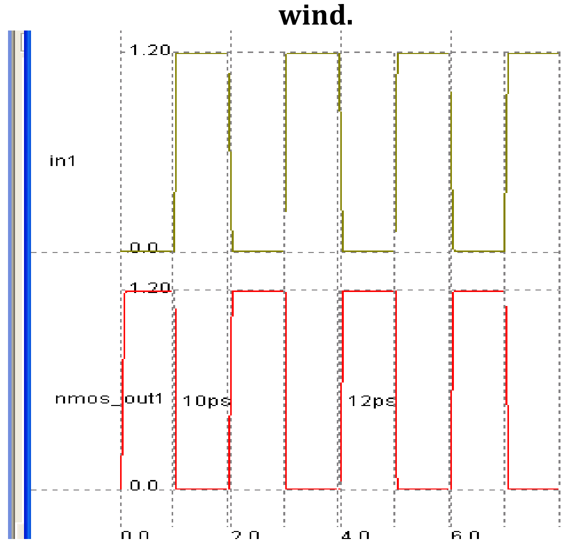

Figure 9,10 shows Inverter characteristics

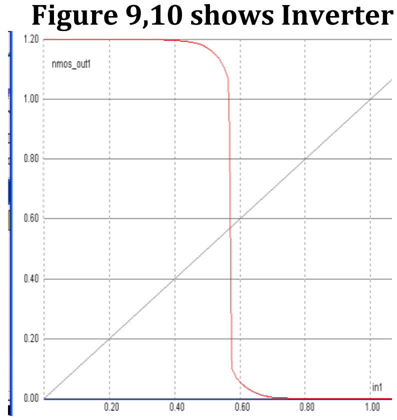

Figure 10 Inverter characteristics

Figure 8 shows Layout schematic of CMOS 0.12 µm technology. Figure 9 and 10 shows IN and OUT characteristics. Table III gives Parameters and its values of CMOS.

S.NO	Parameter	Values
1	AREA	50 μm^2
2	SPEED	20 ns
3	FREQ	0.05 GHZ
4	POW DISSIP	0.054 mW
5	W/ L	1.9 / 0.12
6	I max	0.325 mA

Table III Inverter values

4.3 COMPARISON

From Table II and III it is found that in area and speed wise QCA circuits are better than CMOS circuits. The area of QCA INVERTER is 5000 nm^2 and that of CMOS 50 μm^2, nearly 10 times area can be saved. Similarly speed wise one-third speed is increased in QCA circuits.

5 STUDY II

5.1 QCA CIRCUIT – NAND & NOR

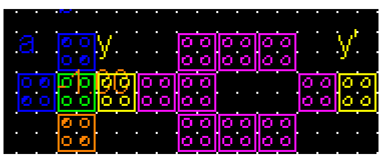

Figure 11 a – QCA NAND [6]

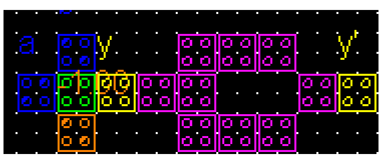

Figure 11 b – QCA NOR[6]

Figure 11 a and b gives QCA Nand and Nor Circuits. The difference between a and b circuits being Control signal = 0 (-1) for Nand and 1 (+1) for Nor circuit. Figure 12.a and b shows the simulation of 11.a and b QCA circuits. The output Y' of 11.a and b is available at clock 2.Clock 1 is used to find AND and OR logic (y).

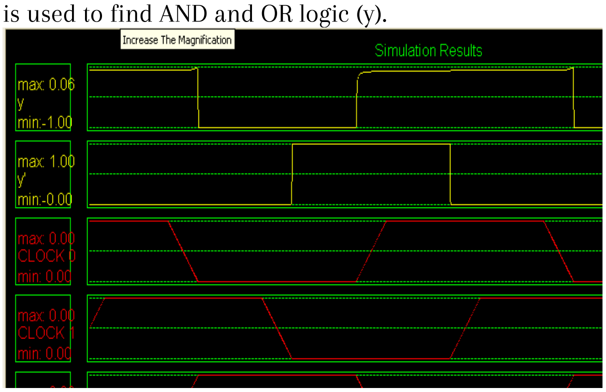

Figure 12 a simulated waveform of QCA NAND

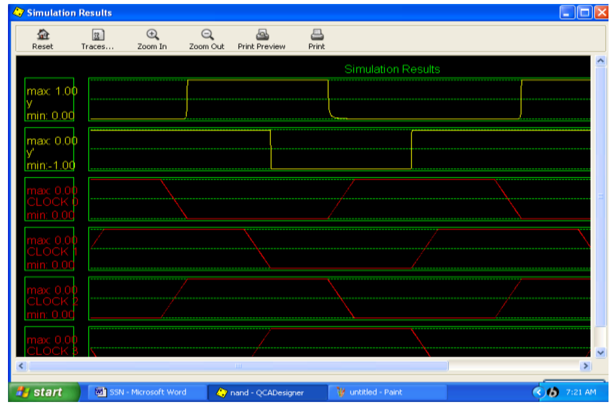

Figure 12 b simulated waveform of QCA NOR.

For the above both the diagrams, output is available at clock2. The input for NAND circuit is a = 1 and b = 0 and output y' = 1. The input for NOR circuit is a = 1 and b = 1 and output y' = 0

.

Table IV gives Parameter and their values of ACA Nand and NOR circuit.

S.NO	PARAMETERS	NAND	NOR
1	Speed	12 ns	12 ns
2	Area	6000 nm^2	6000 nm^2
3	Radius	80 nm	80 nm
4	Temperature	5 k	5 k
5	Clk high	9.8 E –21	9.8 E –21
6	Clk low	3.7 E –22	3.7 E – 22
7	No of cells	15 QCA	15 QCA

Table IV Parameters and their values of QCA Nand and Nor Circuits.

5.2 CMOS NAND & NOR CIRCUITS

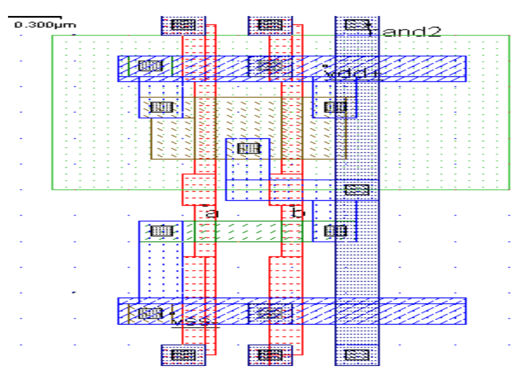

Figure 13 a CMOS Layout for Nand circuit,

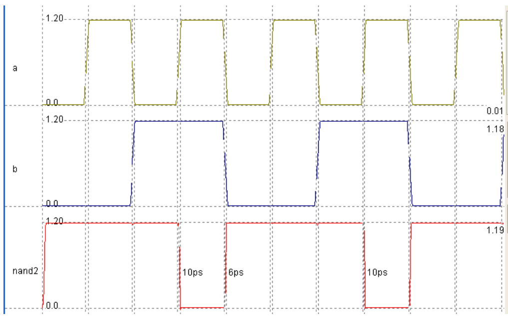

Figure 13 b Simulated waveforms of NAND

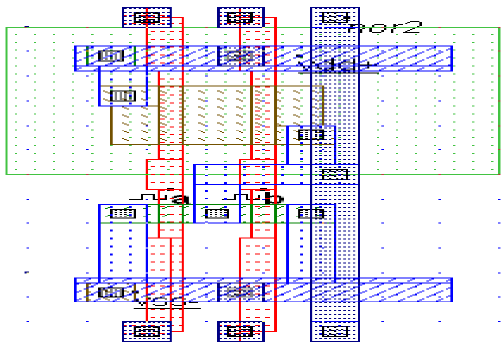

Figure 14 a CMOS NOR circuit.

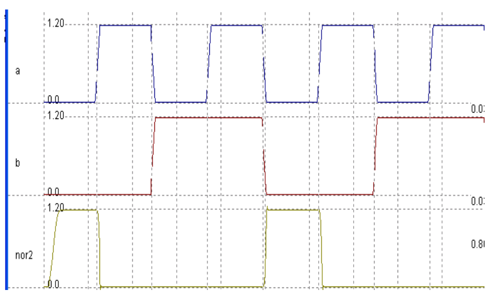

Figure 14 b Simulated waveform of NOR circuit.

Figure 13 and 14 shows CMOS NAND and NOR circuits and their waveforms. Table V shows the CMOS NAND and NOR Parameters and their Values.

S.NO	PARAMETERS	NAND	NOR
1	SIZE	150 μm^2	160 μm^2
2	SPEED	40 ns	42 ns
3	FREQ	2.5 Mhz	2.56 Mhz
4	Ileak	0.1 ma	0.2 ma
5	W / L	0.24 / .12	0.2 /0.12
6	POWER DISSIPTION	0.685 mW	0.186 mW

Table V CMOS Nand and Nor Parameters and values

5.c. COMPARISON OF QCA & CMOS CIRCUITS

It is noted that from figure 11 to 14 and Table V and IV, QCA circuit having less area and higher speed than CMOS circuits. However the Power dissipation in QCA circuit is related with Clock high and low (latching). The values of Clk high and low are negligibly small, no need for comparison on power dissipation in case of QCA circuit.

6. STUDY III – FULL ADDER CIRCUITS

6.1 QCA FULL ADDER CIRCUIT

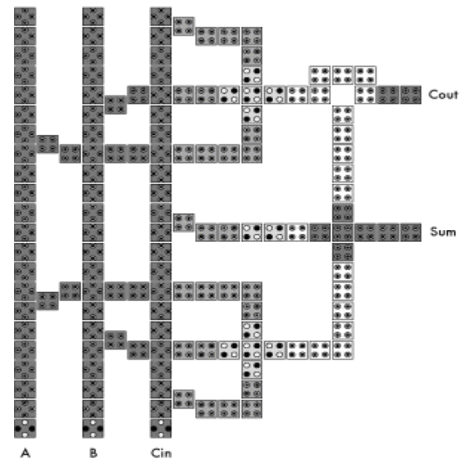

Figure 15.a QCA FULL ADDER [3]

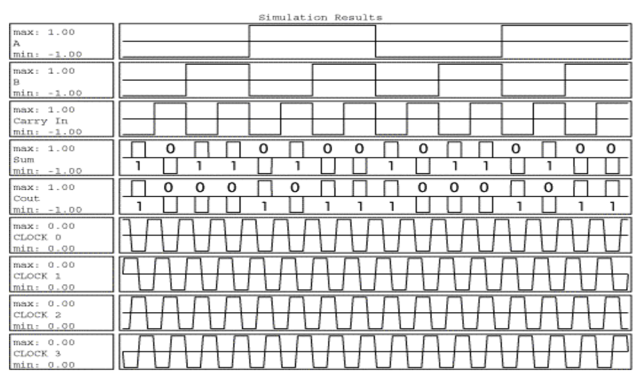

Figure 15.b Simulation of QCA FULL ADDER

Figure 15 shows the QCA full adder, During Clock 0 the output Sum and Carry is evaluated. When clock 0 goes low the output sum = 0 when a, b, c =0. In QCA circuits output available during next clock phase.

6.2 CMOS FULLADDER

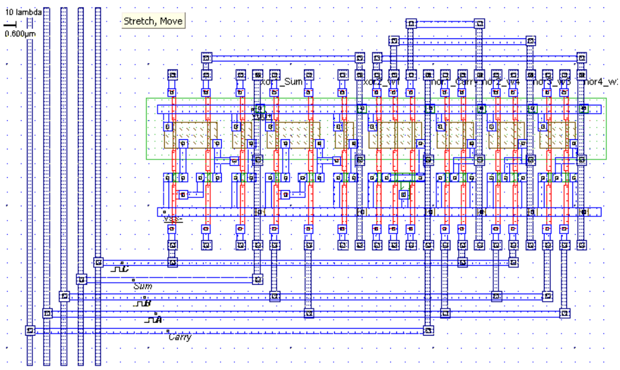

Figure 16.a CMOS full adder [7]

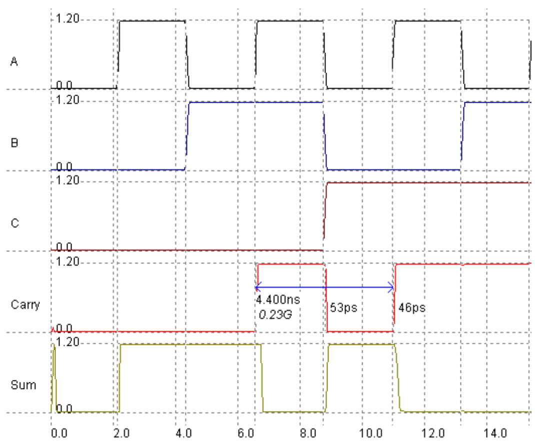

Figure 16.b Simulated Waveform

Figure 16 shows CMOS Full adder layout and its simulated waveform.[7]

6.3 COMPARISON

S.NO	PARAMETER	QCA FA	CMOS FA
1	Area	160 µm²	400 µm²
2	Speed	80 ns	150 ns
3	Temp	5 k	27 ºC
4	Pow.diss	-	0.543 mW
5	W / L (CMOS)	Total 82 cells	0.36 / 0.12

Table VI parameters and values of QCA and CMOS circuits

From the table it is found that Area and speed wise QCA circuits are best and this technology can be used.

7.1 ADVANTAGES OF QCA OVER CMOS

1. High packing density (10^{10} / cm^2 cells)
2. Very low power dissipation (10^{-10} W [per unit)
3. Compatibility with nanostructures
4. High computational speeds.
5. Routing, Interconnection between cells are easy[1][2]

7.2 DRAWBACKS

1. 1.Prescence of Metastable state which the system is trapped infinite amount of time [6].
2. Technology operated in Cryogenic temperature [1,2].

8. CONCLUSION

QCA technology is a nano technology, which plays important role in the future. In this paper CMOS circuits are compared with QCA circuits, Since QCA circuits are built in cells of nanometer size, these circuits gives high speed and utilizes lesser area. Therefore today CMOS drawbacks can be avoided by switching to QCA technology. But further drawbacks of QCA circuits can be avoided by moving to molecular QCA technology [5]. Since the above technology is in research a long way to go for further development. Further we can develop a theoretical processor model using QCAD and also some of the algorithms also been developed.

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