"DESIGN A 128-BIT VEDIC MULTIPLIER"

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ABSTRACT

Vedic arithmetic is that the name given to the traditional Indian system of arithmetic that was rediscovered within the early twentieth century from ancient Indian sculptures (Vedas). This paper proposes the planning of high-speed religious writing number mistreatment the techniques of religious writing arithmetic that are changed to boost performance. A high-speed processor depends greatly on the number because it is one in every of the key hardware blocks in most digital signal process systems further as normally processors. religious writing arithmetic includes a distinctive technique of calculations supported sixteen Sutras. This paper presents study on high speed 128x128 bit religious writing number design that is sort of totally different from the standard technique of multiplication like add and shift. As the multiplier provides 256 bit of output. The design is developed on vhdl language.

KEYWORDS: *vhdl (VHSIC Hardware Description Language)*

I. INTRODUCTION

Multiplication based operation such as multiply and accumulated and inner product are among some of the frequently used Computation - Intensive Arithmetic Functions currently implemented in many Digital Signal Processing applications such as convolution, Fast Fourier transform, filtering and in microprocessors in its arithmetic and logic unit. Vedic multiplier uses Vedic sutras. Word 'Veda' stands for 'knowledge' in Sanskrit. Vedic mathematics is conceived to be rebuild from Vedas by Sri Bharti Krishna Tirathaji between the years 1911 to 1918 The Vedic mathematics has been divided into sixteen different Sutras which can be applied to any branch of mathematics like algebra, trigonometry, geometry etc. Its methods reduce the complex calculations into simpler ones because they are based on methods similar to working of human mind thereby making them easier. It has been seen that being coherent and proportional, they take minimum power and take lower chip area. Vedic Mathematics deals with Sixteen Sutras. These sutras are given below alphabetically with their brief meaning. All these sutras have huge study.

II. METHODOLOGY
Proposed work

Vedic mathematics is part of four Vedas (books of wisdom). It is part of Sthapatya- Veda (book on civil engineering and architecture), which is an upa-veda (supplement) of Atharva Veda. It gives explanation of several mathematical terms including arithmetic, geometry (plane, co-ordinate), trigonometry, quadratic equations, factorization and even calculus.

In vedic mathematic two sutras are dedicatedly used for multiplication functions. One is Nikhilam Navatascaramam Dasatah sutra and other is Urdhva–Tiryagbhyam sutra. Our focus is only on the Urdhva–tiryagbhyam sutra as in the Nikhilam Navatascaramam Dasatah sutra, multiplier and multiplicand both are required to be nearer to bases of 10, 100, 1000 that is increased powers of 10. The sixteen sutras of Vedic mathematics and their meaning are listed in Table 1.

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Table 1: List of Vedic sutras.

Sr no	Sutras	Meaning
1	Ekadhikena purvena	By one more than previous one(division)
2	Nikhilam navatascaramam	All from nine and last from ten(multiplication)
3	Urdhva tiryagbhyam	Vertically and crosswise (multiplication)
4	Paravartya yojayet	Transpose and adjust (division of polynomial equation)
5	Sunyam sayasamuccaye	When the sum is the same that sum is zero
6	Sunyamanyat	If one is in ratio, the other is zero
7	Sankalana-vyavakalanabhyam	By addition and by subtraction
8	Puranapuranabhyam	By the completion and non-completion
9	Calana kalanabhyam	Differences and similarities
10	Yavadunam	Whatever the extent of deficiency
11	Vyastisamastih	Part and whole
12	Sesanyankena caramena	The remainders by the last digit
13	Sopantyadvayamantyam	The ultimate and twice the penultimate
14	Ekanyunena purvena	By one less than the previous one
15	Gunitasamuccayah	The product of the sum is equal to the sum of the product
16	gunakasamuccayah	The factors of the sum is equal to the sum of the factors

Figure2 shows *the* the steps required for multiplication by using Urdhva-Tiryagbhyam sutra. For this we consider the multiplication example of 576 *x* 324. From figure 2 first multiply the left most digit 6 of the multiplicand vertically by the left most digit 4 and it gives the result as 24 from that result product 4 and carry 2 set down as the left hand most part of the answer; then multiply 7 *x* 4 and 6 *x* 2 crosswise and add them get 40 and add carry 2 from previous as the sum set it down as the middle part of the answer and so on. Lastly, we get the result as 576 *x* 324 = 186624
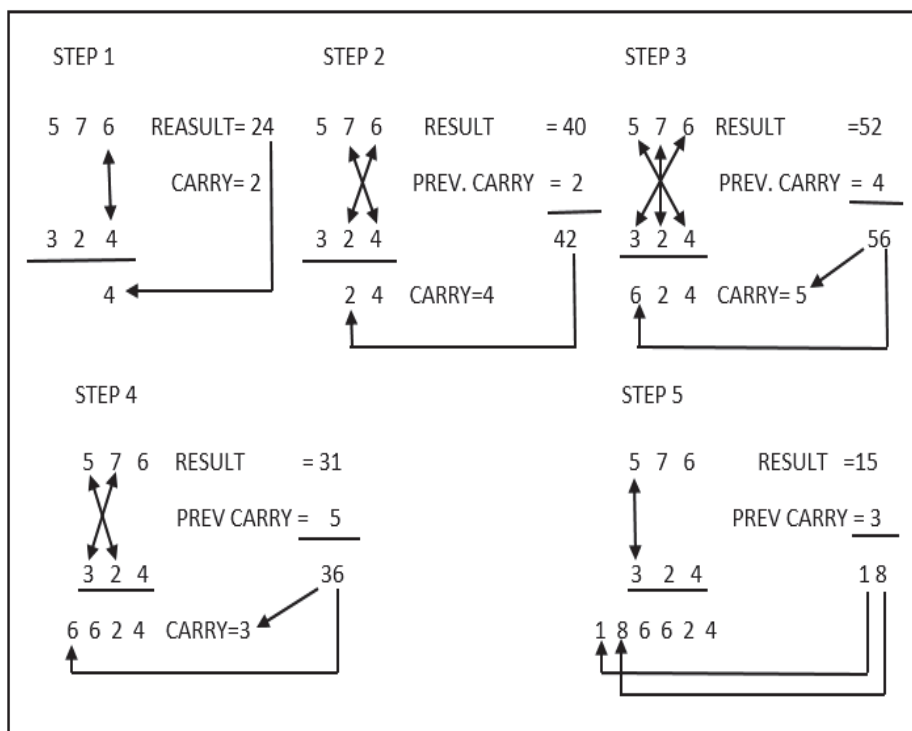
Fig(2)

III.   TOOLS REQUIRED
Software tools

1   **XilinxISE:**

   Integrated **S**ynthesis Environment) is   a software   tool   produced   by Xilinx for synthesis   and   analysis of HDL designs, enabling   the   developer to synthesize ("compile") their designs, perform timing analysis, examine RTL diagrams, simulate a design's reaction to different stimuli, and configure   the   target   device   with the programmer.

2   The Xilinx ISE is a design environment for FPGA products from Xilinx, and is tightly-coupled to the architecture of such chips, and cannot be used with FPGA products from other vendors. The Xilinx ISE is primarily used for circuit synthesis and design, Other components shipped with the Xilinx   ISE   include   the   Embedded Development Kit (EDK), a Software Development Kit (SDK) and Chip Scope Pro.

IV.   RESULTS AND CONCLUSION
Device utilization

Following subsections presents the device utilization and memory requirement

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice LUTs	36247	19200	188%
Number of fully used Bit Slices	0	36247	0%
Number of bonded IOBs	512	220	232%

Delay:

   Total delay: 23.056ns
   Logic   delay: 12.411ns
   Route   delay: 10.645ns route

   Top level entity of 64-bit BIST FOR VEDIC MULTIPLIER

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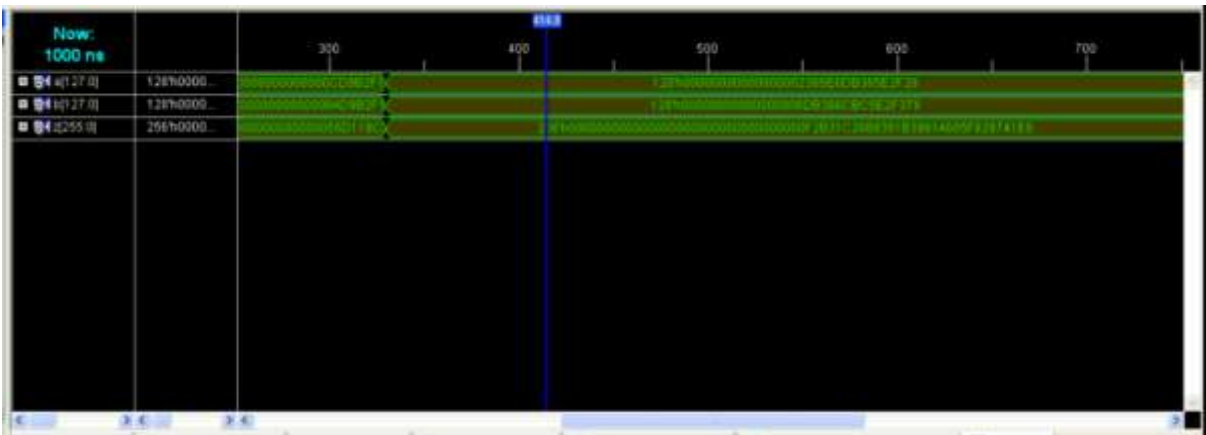
SIMULATION RESULTS OF 128X128 BITS VEDIC MULTIPLIER

a   : Input data 128 – bit

b   : Input data 128 – bit

z   : Output data 256- bit

a = 128'h

b = 128'h

y =256'h0F2B31C2889351B3981A005F829741E

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