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SUBTHRESHOLD CONDITION IN MOSFET

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ABSTRACT

Sub-threshold conduction is an important consideration when dealing with modern devices, especially due to the trend towards increasingly smaller device sizes. Shorter channels have adverse effects on sub-threshold swing, affecting device operation in this region. Analog designers would like a smooth and accurate model in order to properly utilize this highly efficient operating region, while digital designers would prefer to understand methods to minimize channel conduction when a device is in sub-threshold. This paper will review previously published works that discuss analytical models for different sub-threshold concerns, including short-channel effects and the effects due to barrier-lowering. Experimental data is also presented which verifies some of these selected models. Finally, areas for further research into this operating region will be presented.

INTRODUCTIONS

Now a days the sub-threshold region of MOSFETs is a part of interest for both analog and digital designers sub-threshold region is where the transistor operation in weak inversion mode i.e. a bit below threshold voltage ($V_{GS}<V_T$). Working at this region is useful for systems that should work at low voltages around 1V. sub-threshold operation has several desirable characterstics, there are several benefits of sub-threshold region like In analog applications, sub-threshold gives high gain, and in digital applications, it can gives the high ON/OFF ratio. The main benefit working at this region is that the output current is related exponentially with the input voltage rather than the quadratic relationship to the input voltage in saturation region. This increases the trans-conductance of the MOSFET and so getting higher gain. It is hard to say where this region start for sure but a 50mV less than the threshold voltage is good.

THEORY

Sub-threshold conduction is characterized by a current flow in the case when ($V_{GS}< V_T$). Generally the current-voltage relationship which is used in simple design predicts zero current when ($V_{GS}<V_T$), but the drain current (I_D) is not practically be zero when ($V_{GS}<V_T$) .Fig. 1 shows a comparison between the ideal characteristics and the sub threshold characterstics.

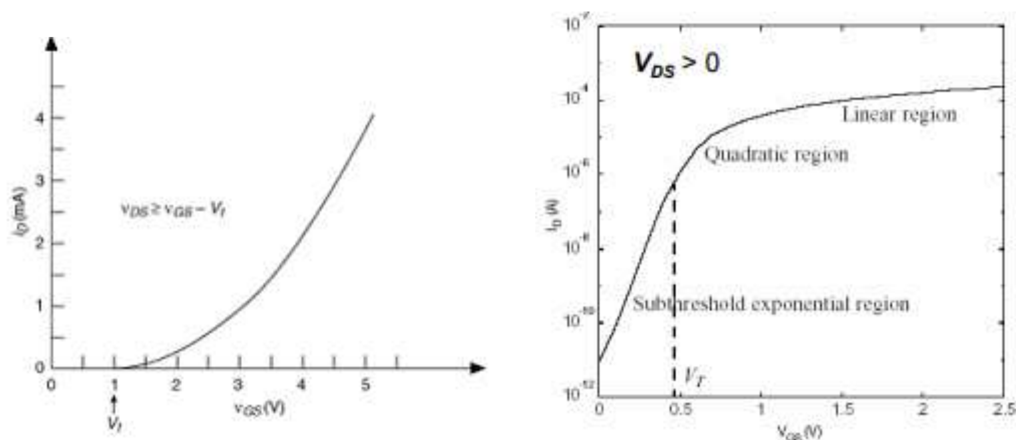

Fig. 1 comparison between the super-threshold characteristics and the sub-threshold characterstics.

The sub-threshold condition occurs when MOSFET is biased in weak inversion mode, Fig. 2 shows the energy-band diagram of a MOS structure with a p-type substrate biased so that $\varphi_s < 2\varphi_B$, due to this biasing the Fermi level comes closer to the conduction band than that of the valence band at the interface between the gate-substrate interface and at the interfaces the semiconductor develops the characteristics of a lightly doped n-type material and small amount of conduction will occurs and this conduction is due to the diffusion of minority carriers in the n-channel.

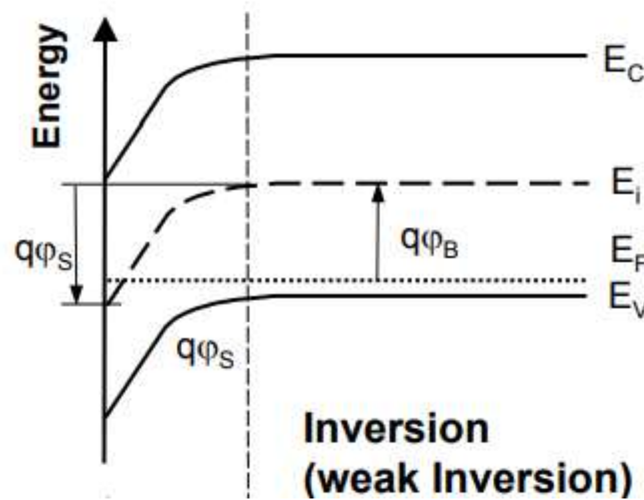

Fig. 2 shows the energy-band diagram of a MOS structure with a p-type substrate in weak inversion mode.

An important parameter when discussing sub-threshold conduction is called sub-threshold slope.The sub-threshold slope S is an important parameter to study about the sub-threshold conduction and It is defined as the amount of gate voltage required to change the drain current (I_D) by 1-decade. Fig. 3 shows the sub-threshold slope in sub-threshold condition with respect to V_{GS}

$$S = (\partial V_{GS}/\partial \log I_D)$$

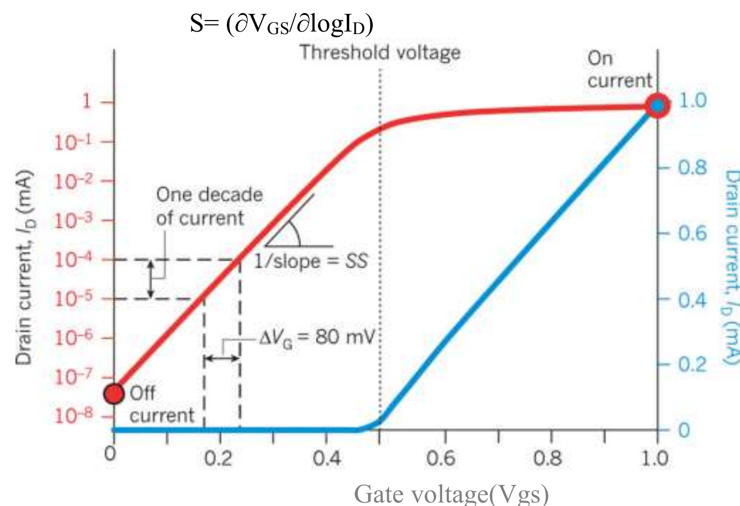

Fig. 3 shows the sub-threshold slope in sub-threshold condition with respect to V_{GS}

For V_T ~26 mV (room temperature) and the ideal case of n=1, the ideal sub-threshold slope for MOSFETs is ~60mV/decade. However, the feasible slopes are around 70~80 mV/decade. Furthermore, as temperature increases, so does V_T and the sub-threshold slope.

Sub-threshold slope is a very crucial parameter which represent ON-OFF switching capability of

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MOSFET. Larger values of Sub-threshold slope would implies better I_{ON}/I_{OFF} due to this power dissipation will reduces.

The Sub-threshold slope is also defined as the reciprocal of the Sub-threshold swing:-

$$SS= (\partial \log I_D/\partial V_{GS})^{-1}$$

This implies that to get better I_{ON}/I_{OFF} Sub-threshold swing must be smaller.

FACTOR AFFECTING THE SUB-THRESHOLD SWING

1. DOPPING

Fig. 3 shows that SS decreases with increasing doping this takes place as the doping is increases the effective conduction path shift towards the gate, which leads to better control on the gate over current conduction. Thus, a MOSFET with higher doping behaves as a better switch. This result can also be confirmed by the I_{ON} /I_{OFF} ratios which increase with an increase in channel doping.

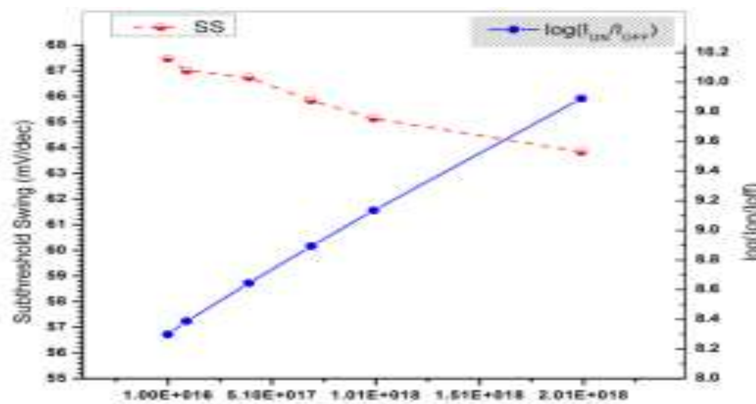

Fig. 3 shows that SS decreases with increasing doping

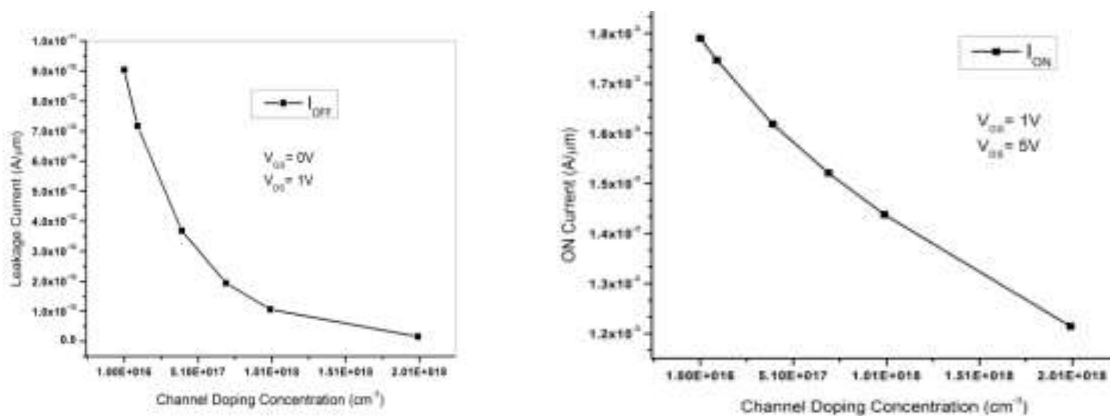

Fig. 4 shows the behaviour of I_{OFF} andI_{ON} with increasing doping

2.TEMPRATURE

At room temprature the ideal value of the SS is 60 mv/dec but as we know that the device actually works on the temprature greater than the ambient temprature due to heat dissipation so the value os SS will be higher as tempreture increases and lower down significantly as tempreture decreases due this we can say that the SS is directly proportional to the tempreture moreover the threshold voltage increases when temperature decreases. Because, when temperature decreases carriers in the channel become freeze. Hence higher gate voltage is required to invert the channel. Therefore, subthreshold drain current can be increased by lowering the temperature.

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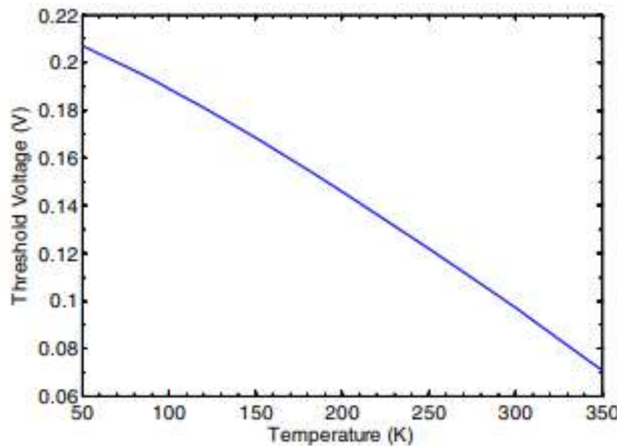


Fig. 4 shows the behaviour of threshold voltage withrespect to the temprature(K)

3. SUBSTRATE BIASING

As the substrate biasing is applied then due this substrate biasing the SS is increasing and hence threshold voltage decreases.

MOSFET AMPLIFIER OPERATION IN SUB THRESHOLD REGIME

The benefit of operating the MOSFET transistor in the subthreshold region is that the transistor input capacitance in the subthreshold region is much less than that of the superthreshold region. On the other hand, the input capacitance in the superthreshold operation is dominated by the gate-oxide capacitance. Due to the smaller input capacitance and the lower-supply voltage in the subthreshold region, the power consumption will be much less than that in the superthreshold region. The subthreshold region operation was investigated and utilized especially in digital-circuit applications.

The following Equation is the current-voltage relationship for the sub-threshold transistor:-

$$i_{sub} = I_0 e^{\frac{v_{GS} - V_{th0} - \gamma v_{SB} + \eta v_{DS}}{n V_T}} \left(1 - e^{-\frac{v_{DS}}{V_T}}\right)$$ ……….(1)

Where $I_0 = \mu_0 C_{ox} \left(\frac{W}{L}\right) V_T^2 e^{1.8}$

where W and L are the transistor channel width and length, respectively, μ0 is the electron mobility at low electric fields, Cox is the gate-oxide capacitance per unit area, VT is the thermal voltage and is given by V_T =KT/q where k is Boltzmann's constant, T is the ambient γγtemperature, and q is the electronic charge, n is the subthreshold swing factor, γ is the linearized body-effect coefficient, η is the drain-induced barrier lowering (DIBL) coefficient, and Vth0 is the threshold voltage at zero source-to-substrate voltage. If the body-effect coefficient and the drain-induced barrier lowering (DIBL) coefficient are neglected, then Eq. 1 can be written simply as:-

$$i_{sub} = I_0 e^{\frac{v_{GS} - V_{th}}{n V_T}} \left(1 - e^{-\frac{v_{DS}}{V_T}}\right)$$ …………..(2)

If the drain-to-source voltage, vDS is larger than 3VT, then we can consider the factor e^{-V_{ds}/V_t} to be much less than 1, and thus Eq. 2 can be written as:-

$$i_{sub} = \mu_0 C_{ox}\left(\frac{W}{L}\right)V_T^2 e^{1.8} e^{\frac{v_{GS}-V_{th}}{nV_T}}$$ ………..(3)

SMALL SIGNAL ANALYSIS OF SUB-THRESHOLD AMPLIFIER

Lets assume the net applied gate voltage is $v_{GS} = V_{GS} + v_{gs}$.
where we have adopted the convention that the voltages or currents with small symbols and large subscripts refer to total voltages or currents and those with capital symbols and subscripts refer to pure dc values and those with small symbols and subscripts refer to pure ac values . In this case, the total value of the subthreshold leakage current will be equal to

$$i_{subt} = \mu_0 C_{ox}\left(\frac{W}{L}\right)V_T^2 e^{1.8} e^{\frac{V_{GS}+v_{gs}-V_{th}}{nV_T}}$$

where isubt is the total (dc+ac) subthreshold current. Expressing the exponential term $e^{v_{gs}}$ in a Taylor-series expansion, we obtain

$$i_{subt} = \mu_0 C_{ox}\left(\frac{W}{L}\right)V_T^2 e^{1.8} e^{\frac{V_{GS}-V_{th}}{nV_T}}$$

$$\left(1 + \frac{v_{gs}}{nV_T} + \left(\frac{v_{gs}}{nV_T}\right)^2 + \left(\frac{v_{gs}}{nV_T}\right)^3 + \ldots\ldots\right)$$

For small ac values of the gate-to-source voltage; that is when vgs<< nVT, we can neglect the second and higher-order terms in the Taylor-series expansion and thus the total subthreshold current, i_{subt} can be expressed as the sum of a dc current and an ac small-signal current of the first order as follows:-

$$i_{subt} = I_{sub} + i_{sub}$$ ……………(4)

$$= \mu_0 C_{ox}\left(\frac{W}{L}\right)V_T^2 e^{1.8} e^{\frac{V_{GS}-V_{th}}{nV_T}}\left(1 + \frac{v_{gs}}{nV_T}\right)$$ ……………(5)

$$= I_{sub} + \frac{I_{sub}}{nV_T} v_{gs}$$ ……………(6)

$$\therefore i_{subt} = I_{sub} + g_m v_{gs}$$ ……………(7)

where g_m represents the transconductance of the subthreshold transistor and is given by:-

$$g_m = \frac{I_{sub}}{nV_T} \quad \text{………….(8)}$$

The term small-signal needs to be more clarified. In fact, the higher-order terms such as

$$\left(\frac{v_{gs}}{nV_T}\right)^2 \text{ and } \left(\frac{v_{gs}}{nV_T}\right)^3, \ldots$$

etc can be neglected only if the ac small-signal voltage, vgs is less than one tenth the value of nV_T. Depending on the values of n and V_T, the maximum amplitude of the ac gate-to-source voltage for linear operation can be determined. This is less than its counterpart in the superthreshold device where the maximum permissible value for vgs is dictated by the following inequality:-

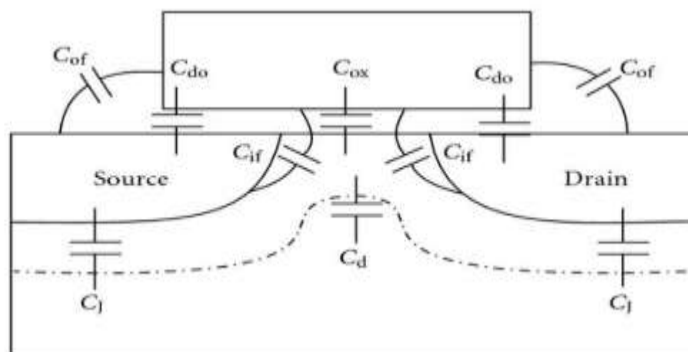
$$v_{gs} << 2(V_{GS} - V_{th})$$

There is one drawback of operating MOSFET in sub-threshold region, the value of g_m of the subthreshold transistor is much less than that of the conventional MOSFET device. This also comes to no surprise because the subthreshold current is much less than the drain current in the superthreshold region. So, we can expect that the voltage gain of the subthreshold transistor amplifier is less than that of the superthreshold transistor amplifier for the same load.

FUTURE SCOPE

In the subthreshold region, the transistor input capacitance is less than that of strong inversion operation. The transistor input capacitance (Ci) in subthreshold, is a combination of intrinsic (oxide capacitance(Cox) and depletion capacitance (Cd)) and parasitic (overlap capacitance (Cdo) , fringing capacitances((Cif , Cof)) of a transistor (Figure 1) and is given by :-

$$C_i = \text{series } (C_{ox}, C_d) \| C_{if} \| C_{of} \| C_{do}.$$



In contrast, the input capacitance in strong inversion operation is dominated by the oxide capacitance. Due to the smaller capacitance and lower supply voltage (< threshold voltage of the transistor), digital subthreshold circuits consume less power than their strong inversion counterpart at a particular frequency of operation. Sub-threshold circuits can minimize energy for computations executed during the low-performance slots.This application of sub-threshold can be used in high-performance microprocessors, cell phones etc.

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