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A REDUCED SWITCH THIRTEEN LEVEL INVERTER FOR PHOTOVOLTAIC APPLICATIONS

Mr.A.VinothKumar[1]
[1]*Assistant Professor EEE, P A College of Engineering and Technology. Pollachi*

Dr.S.Vijayabaskar[2]
[2]*Head of the Department, EEE, P A College of Engineering and Technology. Pollachi*

Ms.C.Selsiya[3]
[3]*Assistant Professor EEE, P A College of Engineering and Technology. Pollachi*

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ABSTRACT

The demand for clean and sustainable energy has prompted research into all types of renewable energy sources, including solar energy generated by photovoltaic systems. We suggest a new multi level inverter topology in this paper. This paper looks at a PV-based 13-level multi level inverter with fewer switches. The most gainful power converters for high power applications and modern applications with fewer switches are multi levelinverters. PWM methodology is used to manage the proposed topology. The proposed topology has one of the highest efficiency and lower voltage THD. The inverter produces output voltage in thirteen levels: Vdc, Vdc/2, Vdc/3, Vdc/4, Vdc/5, Vdc/6, 0, -Vdc, -Vdc/2, -Vdc/3, -Vdc/4, -Vdc/5 and -Vdc/6. The validity of the proposed inverter is verified through simulation.

KEY WORDS: *Pulse Width modulation (PWM), Photo Voltaic (PV) Source.*

1. INTRODUCTION

The PV inverter, the brains of a PV system, converts dc power from PV modules into ac power that can be fed into the grid. The size of the filter used and the degree of Electromagnetic Interference (EMI) produced by switching operation of the inverter are reduced when the output waveform of the inverter is improved. Because of their advantages over traditional PWM inverters, multi level inverter shave become more appealing to researchers and manufacturers in recent years.

They have better output waveforms, a smaller filter size, and lower EMI as well as lower Total Harmonic Distortion (THD)[1].

2 PHOTOVOLTAIC SYSTEM

The DC supply from the solar panel is used to power this multi level inverter. For example, a 10 watt panel has a voltage of 17.6 and a current of 0.56A. A solar cell is the most basic part of a solar PV system. Solar modules are made up of solar cell assemblies. Solar panels and sun-based boards are made up of a large number of solar modules. Figure 1 demonstrates the corresponding circuit for a photovoltaic module.

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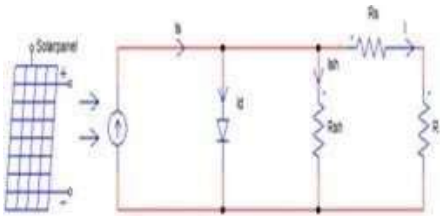

Fig1.Equivalent circuit of solar panel

This sun-oriented cell has little to do with the inverter and diode that are connected in parallel. This current source is said to be parallel to the diode and shunt resistance. Id-Diode current, Is-dispersion current, T-incomparable temperature Boltzmann compatible (1.38051023J/K), Charge q =1.6 1019 C are the yield curves of the sun-oriented cell. Regarding the fabricate misfortunes, the PV cell's identical circuit consists of two resistances Rs and Rp connected in series and parallel, where Rs represents the misfortunes caused by contacts and interactions and Rsh represents the spillage streams in the diode as defined.

3 PULSE WIDTH MODULATION

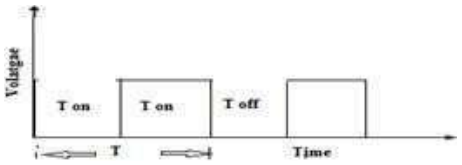

Fig2. Pulse width modulation Technique of the proposed system

As seen in figure 2, the Pulse creator is depicted as the turn ON time for the entire day and era, which is referred to as the duty stage. To send the message pulse to the Switches, central pulse plan frame works were used. The ON time is constant in relation to the total voltage conveyed. The switch movement encircles the beats to create a ventured waveform. In this case, 8 switches are switched on to create a 13-level yield waveform [4]. The beat generator uses an OR entry way to create positive voltage waveforms, while an invert gate delivers negative voltage ventured waveforms. Giving the power the entry way pulse is an important technique.

4 CONVENTIONAL SYSTEMS

The traditional 13-level inverter is depicted in the diagram. There are three series. One dc source is connected to seven capacitors and six switches in the traditional topology, as well as one H-bridge with four switches. This circuit uses ten switches in total to produce a thirteen-level output voltage waveform, and it employs a time frame switching scheme to generate output voltage with a sine wave as a reference. In the conventional method, each stage of the output voltage can be obtained by adding and reducing the capacitor in the thirteen level inverter.

This can be tested and tentatively verified using a tangle lab reenactment. The switches in this system are enabled by a Sinusoidal heartbeat width balance. The sinusoidal Pulse balance was generated by contrasting reference and vocation flags, and we have considered inverter topology just as it is discussed in. The H-one extension's leg can be removed from this structure, and the proposed framework will be discussed in the following chapter.

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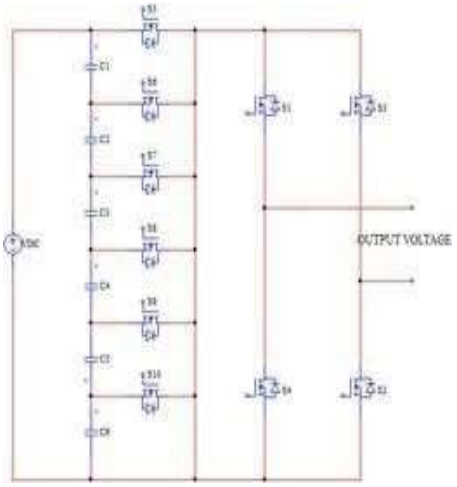

Fig.3.Conventional Thirteen level Multi level inverter

5 PROPOSED SYSTEM

The figure depicts a PV-based 13-level symmetric Multi level inverter. The proposed topology has eight switches, while traditional topologies have ten, making this circuit's thermal stress and operating time superior to conventional systems. The switches in this system are switched using simple pulse width modulation. The proposed inverter has a better total harmonic than traditional systems. The PIC30f2010 microcontroller is used to produce pulses for switches.

Since the carrier has a fixed duration, the switches have a fixed switching frequency. The crossing of the carrier and the modulating signal determines the switching moment

The inverter's switching operation is shown in table 1. Vdc, Vdc/2, Vdc/3,Vdc/4, Vdc/5, Vdc/6,0, -Vdc,- Vdc/2,- Vdc/3, -Vdc/4, -Vdc/5, and -Vdc/6 are the voltage levels in the truth table. The switches' switching operation for the above voltage levels will be on (1) or off (0) depending on the input needed. The input for the pulse width modulation technique can be given as shown in table 1. on and offcan be managed based on the performance required[8].

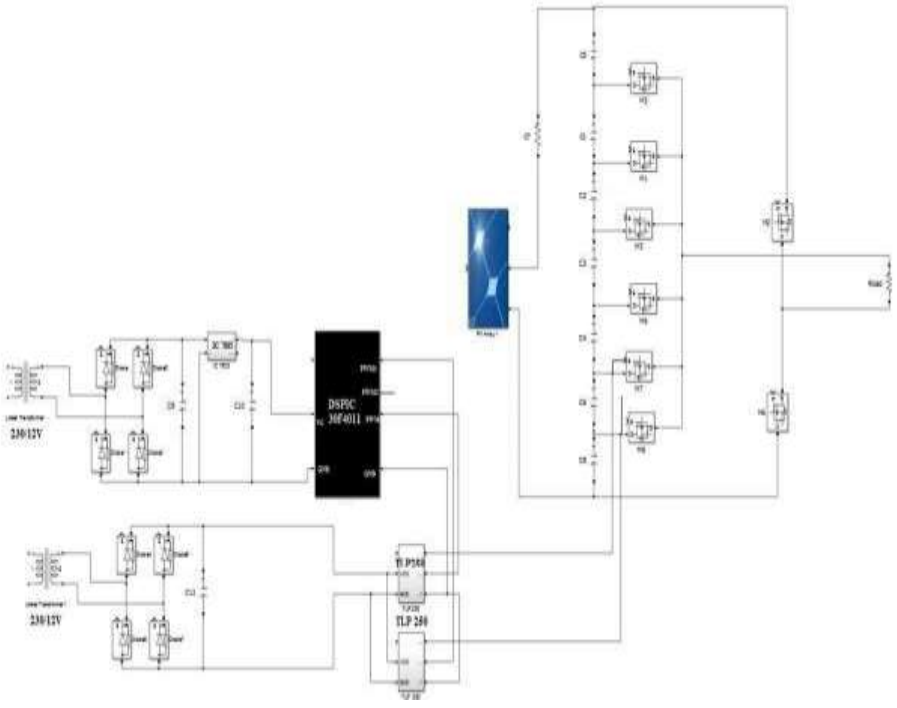

Fig.4.Proposed Multi level inverter

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Table.1Truth table for the multi level inverter

LEVELS	S1	S2	S3	S4	S5	S6	S7	S8
Vdc	0	1	0	0	0	0	0	1
2Vdc	0	1	0	0	0	0	1	0
3Vdc	0	1	0	0	0	1	0	0
4Vdc	0	1	0	0	1	0	0	0
5Vdc	0	1	0	1	0	0	0	0
6Vdc	0	1	1	0	0	0	0	0
0	0	0	0	0	0	0	0	0
-Vdc	1	0	1	0	0	0	0	0
-2Vdc	1	0	0	1	0	0	0	0
-3Vdc	1	0	0	0	1	0	0	0
-4Vdc	1	0	0	0	0	1	0	0
-5Vdc	1	0	0	0	0	0	1	0
-6Vdc	1	0	0	0	0	0	0	1

6 RESULTS AND DISCUSSION

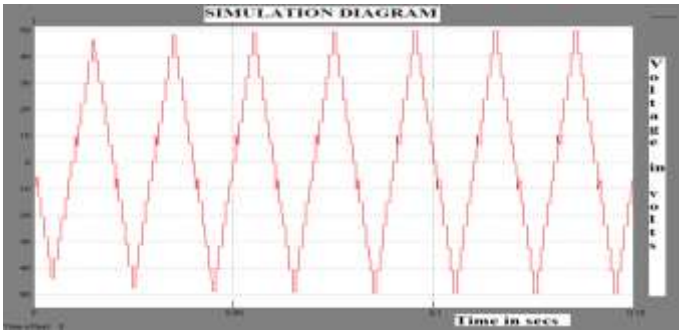

Fig.5 Simulation result for multi level inverter

The proposed inverter developed 13 level stepped waveforms (Vdc, Vdc/2, Vdc/3, Vdc/4, Vdc/5, Vdc/6, 0, -Vdc, -Vdc/2, -Vdc/3, -Vdc/4, -Vdc/5, -Vdc/6) based on the simulation of PV based multi level inverter.

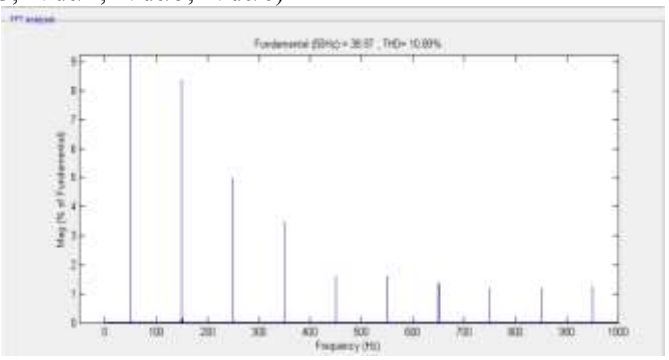

Fig.6 THD Analysis of Proposed Inverter

The proposed thirteen-level multi-level inverter has a total harmonic distortion of
10.89 percent, which is lower than a traditional inverter.

7 EXPERIMENTAL SETUP

The prototype model of multi level inverter as shown in figure. The solar panel is used to give DC

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supply to the inverter.The13level output is obtained from Digital CRO.

Here, we use DSPIC to generate PWM in accordance with our style. To switchon the PIC, we'll need a 5V supply. We use a 230/12V, 1A phase down transformer to step down the grid voltage to 12V AC, then we use a bridge rectifier circuit to convert this 12V AC to 12V dc, and finally we use an IC7805 to convert this 12V dc to 5V dc, and finally we supply this supply to the PIC.

We want a 12V-20V magnitude pulse to turn on the gate of the Mosfet (IRF840), so we used TLP 250 Driver circuit to give 12V DC supply and the 5V pulse that we produced in the PIC, so it will amplify the 5V pulse to 15V Pulse that we will give to the Mosfet. So here we use 8 Mosfet switch, so we need 8-TLP 250 Driver circuit.

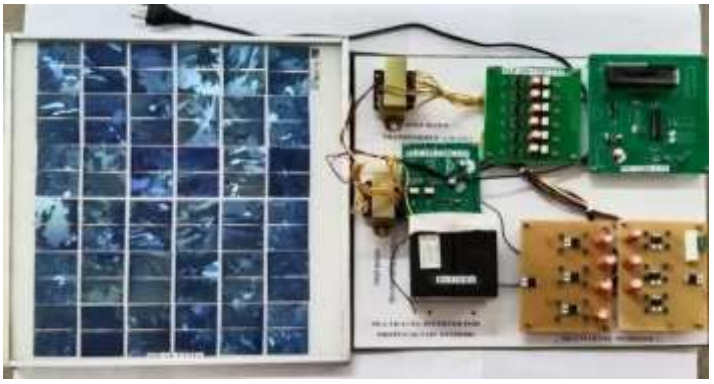

Fig.7.PrototypemodelofPVbased13levelinverter

8 CONCLUSION

Using PWM Technique, a 13-level inverter with less switch expertise is proposed in the proposed methodology. The proposed multi level inverter uses only eight switches to generate a 13-level output waveform from a single DC source, and it can also be used as part of a renewable power source. The proposed multi level inverter was simulated using Mat lab.

9 REFERENCES

1. *S. Daher, J. Schmid, and F. L.M. Antunes, "Multilevel inverter topologies for stand- alone PV systems," IEEE Trans. Ind. Electron., vol. 55, no. 7, pp. 2703–2712, Jul. 2008.*
2. *Kaliamoorthy. M, Sekar R.M., and Rajaram.R, "A new single-phase PV fed five-level inverter topology connected to the grid" IEEE Trans.communication control and computing technologies.pages:196-203, 2010.*
3. *S. Vazquez, J. I. Leon, L. G.Franquelo, J. J. Padilla, and J. M. Carrasco, —DC voltage- ratio control strategy for multilevel cascaded converters fed with a single DC source,‖IEEE Trans. Ind. Electron., vol. 56, no. 7, pp. 2513–2521, Jul. 2009.*
4. *Srinath.K, Dr.P.Linga Reddy, "Matlab/simulink modeling of novel hybrid H-bridge multilevel inverter for PV application" International Journal of Modern Engineering Research., vol.2,issue.2,pp.149-153 March 2012.*
5. *Georgios I.Orfanoudakis, Suleiman M.Sharkh and Michael A.Yuratich, "Analysis of DC- link capacitor losses in three-level neutral point clamped and cascaded H-bridge voltage source inverters."*
6. *V.FernaoPires, J.F.Martins, D.Foito, Chen Hao, "A Grid Connected Photovoltaic System with a Multilevel Inverter and a Le-Blanc Transformer." International Journal of Renewable Energy Research., vol.2, No.1, 2012.*
7. *K.Lakshmi Ganesh, U.Chandra Rao, "Performance of Symmetrical and Asymmetrical Multilevel Inverters", International Journal Mordern Engineering Research., vol.2, issue.4, July-Aug.2012 pp.2293-2302, ISSN: 2249-6645.*
8. *D.PhaniDeepthi, Gandi.Vinaykumar. "A Novel Simplified Single-Phase and Three Phase Multi string Multilevel Inverter Topology for Distributed Energy Resources", International Journal of Engineering Research and Applications", vol.2, issue.3, May-Jun 2012, pp.661-665, ISSN: 2248-9622.*
9. *Divya Subramanian, Rebiya Rasheed, "Five Level Cascaded H-Bridge Multilevel Inverter Using Multicarrier Pulse Width Modulation Technique," International Journal of Engineering and Innovative Technology., vol.3, Issue.1, July 2013.*
10. *Rajesh, M.Balasubramani, J.Gowrishankar, "Newly-Constructed Single Phase Multilevel Inverter for Distributed Energy Resources, "International Journal of Engineering and Technology, vol.5, no.2, Apr-May 2013, ISSN: 0975-4024.*