



H-BRIDGE THIRTEEN LEVEL INVERTER USING REDUCED NUMBER OF SWITCHES FOR INDUSTRIAL APPLICATIONS

¹S.Vijayabaskar, ²D.Subramani, ³K.Manoj and ⁴P.Vishnuprasanth

¹Professor, ^{2,3,4}UG Students

Department of Electrical and Electronics Engineering

P. A. College of Engineering and Technology, Pollachi, Tamil Nadu, India

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ABSTRACT

The single phase cascaded H-bridge multilevel inverter (Thirteen level) is designed for industrial applications and has a decreased number of switches. Cascaded Multilevel Inverters are widely used in the electric utility industry and for industrial motors. When these inverters are used directly for industrial drives, the THD contents in the output voltage of the inverters are extremely important since the performance of the drive is highly dependent on the quality of the voltage applied to it. The symmetric and asymmetric inverters are two forms of cascaded H-bridge inverters that use input voltage from various sources. Only one H-bridge (with four switches) and three additional switches make up the proposed asymmetric cascaded H-bridge topology, which has a total of seven switches for a 13-level output voltage. Drives and renewable energy applications benefit from the new topology. For different layers of multilevel inverters, THD is determined by modulation index. The THD is decreased to 9.18% using the PWM approach, and the THD is analysed using MATLAB/SIMULINK. The proposed topology has been tested utilising a single phase 13 level inverter and a DSPIC 30F2010 controller.

KEYWORD: THD-Total Harmonic Distortion, PWM-Pulse with modulation

I. INTRODUCTION

An electrical power converter that converts direct current (DC) to alternating current (AC) is known as a power inverter (AC). Solid-state inverters are utilised in a broad range of applications, from small computer switching power supply to big electric utility high-voltage direct current applications that transmit bulk power. Inverters are widely used to convert DC electricity from solar panels or batteries into AC power. Normal inverters, on the other hand, have a substantially larger THD. A power inverter is an electrical power converter that transforms direct current (DC) to alternating current (AC). Solid-state inverters are used in a variety of applications, from small computer switching power supplies to large electric utility high-voltage direct current bulk power transmission applications. To convert DC electricity from solar panels or batteries into AC power, inverters are commonly utilised. The THD of normal inverters, on the other hand, is significantly higher. The concept of multilayer converters has been around since 1975. The term "multilevel" comes from the three-level converter. A number of multilayer converter topologies have been developed. The main idea behind a multilayer converter is to complete the power conversion by synthesising a staircase

voltage waveform utilising a series of power semiconductor switches with several lower voltage dc sources. Capacitors, batteries, and renewable energy sources can all be used to provide multiple dc voltage sources. The commutation of the power switches combines these multiple dc sources to produce a high voltage at the output; however, the rated voltage of the power semiconductor switches is solely determined by the rating of the dc voltage sources to which they are attached. Harmonic distortion can cause electrical devices to malfunction. Unwanted distortion in power networks can increase current, resulting in greater temperatures in neutral conductors and distribution transformers. Higher frequency harmonics generate greater core loss in motors, causing the motor core to overheat. Higher order harmonics can interfere with communication transmission lines since they vibrate at the same frequencies as the transmit frequency. If left uncontrolled, increased heat and interference can severely limit the life of electrical equipment and ruin power supplies. As a consequence, the project's number of stages or procedures for reducing THD can be increased.

Ms. Jitha Varghese et al [1] With a contemporary Pulse Width Modulation (PWM) approach, a 13-level



multilevel inverter (MLI) is used. Taghvaie et al [2] The suggested design makes a significant contribution by replacing the isolated DC voltage source with capacitors that are charged at predefined time intervals. Fong et al [3] This work presents a novel architecture of switched-capacitor (SC) Multilevel inverter (MLI) that allows for modular construction. The suggested MLI provides voltage step-up capability and self-balancing of the capacitor voltage by applying the series-parallel SC Technique. Raman et al [4] This paper proposes a family of multiport switched-capacitor multilevel inverter (SCMLI) topologies for high frequency AC power distribution. It employs asymmetric DC voltage sources with a common ground which makes it ideal to be employed in renewable energy farms and modern electric vehicles. Carlos D.Fuentes [5] For large-scale photovoltaic (PV) systems, the multistring configuration is becoming more and more attractive compared with the classical central inverter, since it results in better energy yield by realizing distributed maximum power point tracking. Sajedi et al [6] Performance of multilevel inverters (MLI) are Distinguished because of their low harmonic waveform Generation, low filtering requirements on AC side and high Voltage application.

II. EXISTING METHODOLOGY

In the existing methodology, the thirteen level inverter which is constructed by the switched capacitor multilevel inverter(SCMLI) technique. In this method, it can produce thirteen level output voltage waveform by using eleven switches, three diodes, three capacitors and one DC source. The capacitor voltages are self-balanced as all the three capacitors present in the circuit are connected across the DC source to charge it to the desired voltage level for several instants in one fundamental cycle.

III. PROPOSED SYSTEM

The SCMLI inverter was used to build the proposed single-phase thirteen-level inverter. A single phase conventional H-bridge inverter, three switches, and three voltage sources make up this system. For inverters with the same number of levels, this H-bridge design has considerable advantages over alternative topologies, such as fewer power switches and power diodes. From the dc source voltage, the inverter can generate fifteen output voltage levels (Vdc, 5Vdc/6, 4Vdc/6, 3Vdc/6, and 2Vdc/6, Vdc/6, 0, -Vdc/6, -2Vdc/6, -3Vdc/6, -4Vdc/6, -5Vdc/6, -Vdc).

For this thirteen-level inverter, the MOSFET-based full bridge inverter circuit is cascaded. This h bridge inverter circuit also has three switches linked to it. To protect switching devices against dv/dt and di/dt ratings, a snubber circuit (RC) is linked across all switches. The PWM signals for both the H bridge inverter circuit and the bidirectional switching devices are generated by Spartan 3E. The programme for producing PWM signals will be built utilising the VLSI. The inverter's maximum output power is 10 watts.

The inverter's maximum output voltage level is 72 volts. We can use a bulb or a tiny motor to get this power rating. This project was made into a prototype. From the DC supply, the voltage levels of the thirteen levels are (Vdc, 5Vdc/6, 4Vdc/6, 3Vdc/6, 2Vdc/6, Vdc/6, 0, -Vdc/6, -2Vdc/6, -3Vdc/6, -4Vdc/6, -5Vdc/6, -Vdc). The three sources have varying voltage values. As a result, this setup approach is known as asymmetrical multilevel inverter.

Table 1: 13 level Inverter operation

Voltage Level	S1	S2	S3	H1	H2	H3	H4
Vdc	1	1	1	1	1	0	0
5/6Vdc	1	1	0	1	1	0	0
4/6Vdc	1	0	1	1	1	0	0
3/6Vdc	1	0	0	1	1	0	0
2/6Vdc	0	1	0	1	1	0	0
1/6Vdc	0	0	1	1	1	0	0
0	0	0	0	0	0	1	1
-1/6Vdc	0	0	1	0	0	1	1
-2/6Vdc	0	1	0	0	0	1	1
-3/6Vdc	1	0	0	0	0	1	1
-4/6Vdc	1	0	1	0	0	1	1
-5/6Vdc	1	1	0	0	0	1	1
Vdc	1	1	1	0	0	1	1

Both the modulation index and the inverter's applied DC voltage level determine the inverter's level. We may also increase the number of levels of the inverter by altering the different voltage levels. The PWM signals for the inverter circuit are generated by an FPGA controller. The functioning of the suggested inverter may be separated into thirteen switching states, from which the needed thirteen levels of output voltage were formed. Maximum positive output (Vdc): H1 is turned on, and H2 is turned on, connecting the load positive terminal to Vdc and the load negative terminal to ground. The switches S1, S2, and S3 are turned on. The load terminals are connected to a voltage of Vdc. 5/6 Positive output (5Vdc/6): H1 is turned on, and H2 is turned on, connecting the load positive terminal to Vdc and the load negative terminal to ground. When the switches S1,S3 are turned on, a voltage of 5Vdc/6 is provided to the load terminals. 4/6 Positive output (4Vdc/6): H1 is turned on, and H2 is turned on, connecting the load positive terminal to Vdc and the load negative terminal to ground. The switches S1 and S2,S3 are both turned on. 4Vdc/6 is the voltage supplied to the load terminals. 3/6 Positive output (3Vdc/6): H1 is turned on, and H2 is turned on, connecting the load positive terminal to Vdc and the load negative terminal to ground. The switches S1 and S2,S3 are both turned on. 3Vdc/6 is the voltage supplied to the load terminals. 2/6 Positive output (2Vdc/6): H1 is turned on, and H2 is turned on, connecting the load positive terminal to Vdc and the load negative terminal to ground. The switches S2 and S1,S3 are both turned on. The voltage applied to the load terminals is



2Vdc/6. 1/6 Positive output (1Vdc/6): H1 is ON, connecting the load positive terminal to Vdc, and H2 is ON, connecting the load negative terminal to ground. The switches S3 is ON and S1,S2 is OFF.

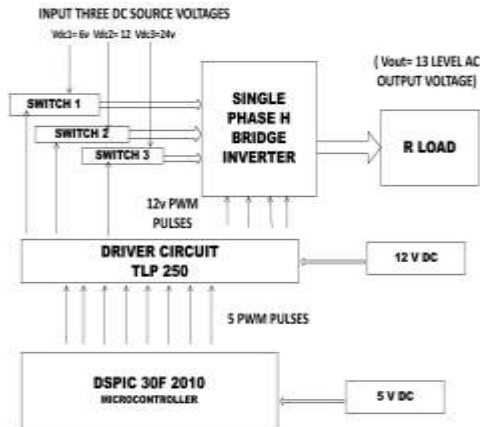


Figure.1 13 level Inverter block diagram

The voltage applied to the load terminals is 1Vdc/6. Zero output: All the switches S1, S2, S3, H1, H2, H3,H4 are in OFF position. 1/6 Negative output (-1Vdc/6): H3 is turned on, and H4 is turned on, connecting the load positive terminal to Vdc and the load negative terminal to ground. The switches S3 and S1,S2 are both turned on. -1Vdc/6 is the voltage supplied to the load terminals. 2/6 Negative output (-2Vdc/6): H3 is turned on, and H4 is turned on, connecting the load positive terminal to Vdc and the load negative terminal to ground. The switches S2 and S1,S3 are both turned on. -2Vdc/6 is the voltage supplied to the load terminals. 3/6 Negative output (-3Vdc/6): H3 is turned on, and H4 is turned on, connecting the load positive terminal to Vdc and the load negative terminal to ground. The switches S1 and S2,S3 are both turned on. -3Vdc/6 is the voltage supplied to the load terminals. 4/6 Negative output (-4Vdc/6): H3 is turned on, and H4 is turned on, connecting the load positive terminal to Vdc and the load negative terminal to ground. The switches S1 and S2,S3 are both turned on. -4Vdc/6 is the voltage supplied to the load terminals. 5/6 Negative output (-5Vdc/6): H3 is turned on, connecting the load positive terminal to Vdc, while H4 is turned on, connecting the load negative terminal to ground. Switches S1,S3 are also turned on. -5Vdc/6 is the voltage supplied to the load terminals. Maximum Negative output (-Vdc): H3 is turned on, and H4 is turned on, connecting the load positive terminal to Vdc and the load negative terminal to ground. The switches S1, S2, and S3 are turned on. -Vdc is the voltage applied to the load terminals.

IV. HARDWARE DESCRIPTION

An inverter is a piece of power electronics that converts DC electricity to AC voltage. Although tiny electrical devices

use DC power, most household appliances use AC power. As a result, we require an efficient method of converting DC power to AC power. A single-phase full-bridge, or H-bridge, inverter is linked to each distinct dc source (SDCS). By connecting the dc source to the ac output using different combinations of the four switches, S1, S2, S3, and S4, each inverter level may provide three distinct voltage outputs, +Vdc, 0, and -Vdc. Switches S1 and S4 are switched on to gain +Vdc, while switches S2 and S3 are turned on to obtain -Vdc. The output voltage is zero when S1 and S2 or S3 and S4 are turned on. The ac outputs of each of the full-bridge inverter levels are linked in series, resulting in a synthetic voltage waveform that is the sum of the inverter outputs. In a cascade inverter, the number of output phase voltage levels m is determined by $m = 2s+1$, where s is the number of independent dc sources.

MOSFETs are semiconductor devices that are commonly utilised in electronic devices for switching and amplifying electronic signals. Because of its compact size, the MOSFET is a core of an integrated circuit that can be developed and produced on a single chip. The source terminal of the MOSFET is typically linked to the body, making it a three-terminal device similar to a field effect transistor. MOSFETs are by far the most prevalent transistor, and they may be found in both analogue and digital circuits. Charge carriers enter the channel through the source and escape through the drain. The voltage on an electrode called the gate, which is placed between the source and drain, controls the channel width. It is protected from the channel by an exceptionally thick layer of insulation.

Gate driver circuit is a circuit that is used to drive power semiconductor devices such as BJTs, IGBTs, and MOSFETs in power electronics converters. The behaviour of gate driver circuits determines the output of DC to DC converters. It means that if the gate driver circuit fails to appropriately drive the gate of the MOSFET device, the output of your intended DC to DC converter will not meet your needs. As a result, while building power electronics converters, the gate driver circuit is crucial.

Microchip Technology's DSPIC Digital Signal Controllers for Motor Control & Power Conversion provide an easy-to-use solution for motor control applications. The DSPIC series of Digital Signal Controllers has a fully integrated digital signal processor (DSP) engine, non-pipelined performance of 30 MIPS, a C compiler-friendly design, and a familiar Microcontroller architecture and design environment. The DSPIC30F2010 devices are divided into three product families: motor control and power conversion, sensor, and general-purpose.

The DSPIC core is a modified Harvard machine with a 16-bit (data) non-pipelined core that combines the control advantages of a high-performance 16-bit Microcontroller with the high computation speed of a fully implemented DSP to produce a tightly coupled, single-chip single-instruction stream solution for embedded systems designs. The original

20-DSPIC30F2010 devices include on-chip secure Flash programme memory space ranging from 12 to 155 kbytes and up to eight kbytes of data space. Many Microcontroller applications require 5 volts of operating power, however many DSPs have a maximum supply voltage of 3.3 volts.

A rectifier is an electrical device that consists of one or more diodes that enable electricity to flow in just one direction. It transforms alternating current into direct current. Furthermore, there are three types of rectifiers: uncontrolled, half-controlled, and fully controlled rectifiers. The rectifier circuit converts alternating electricity to direct current and is often made up of a series of carefully linked diodes. When a diode is connected in series with an alternating current voltage, the negative side of the voltage cycle is eliminated, leaving just positive voltage.

A static electrical power transformer is a device that converts electrical energy from one circuit to another without requiring a direct electrical connection. Mutual induction is used to connect two windings. It transfers power from one circuit to another without affecting the frequency, albeit the voltage levels may change.

Pulse width modulation is the most prevalent and popular digital Pure-sine wave generating technology. The PWM approach entails creating a digital waveform with a duty cycle modified so that the waveform's average voltage corresponds to a pure sine wave. The easiest technique to generate a PWM signal is to compare a low-power reference sine wave to a triangular wave. To create a sinusoidal output wave, multicarrier PWM systems employ high switching frequency carrier waves in relation to the reference waves.

In a typical m-level inverter, m-1 carriers with the same frequency and peak to peak amplitude are used. The amplitude and frequency of the reference or modulation waveform are peak to peak. If the reference waveform is bigger than a carrier signal, the switch/device associated with that carrier is turned on; if the reference waveform is less than carrier signals, the device associated with that carrier is turned off.

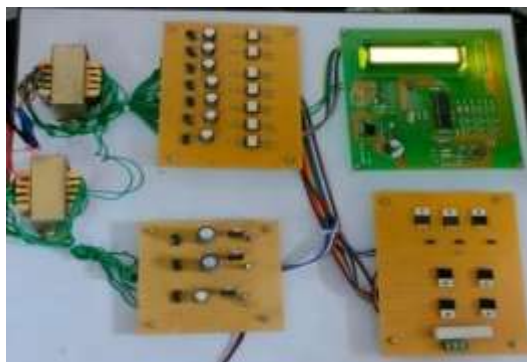


Figure.2 Hardware Picture

V. SIMULATION

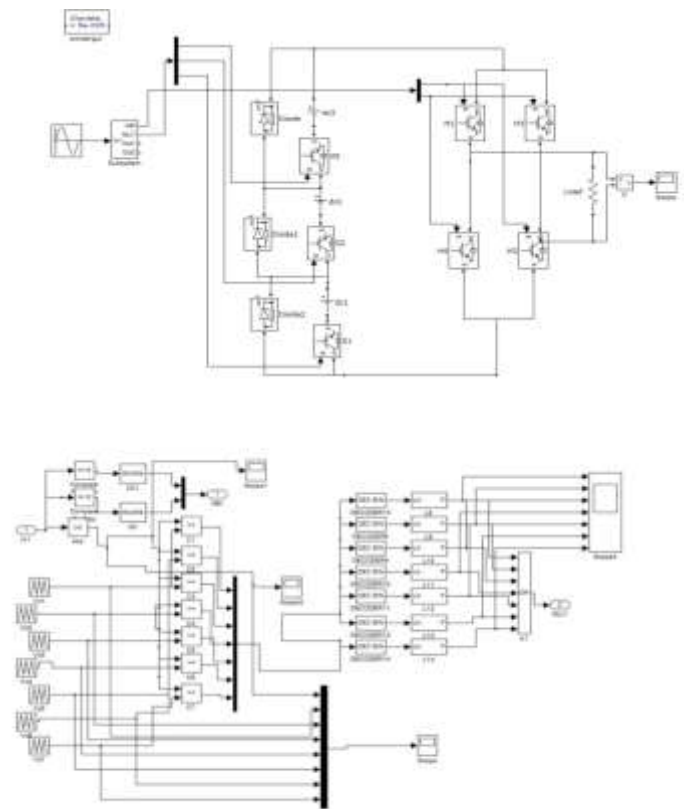
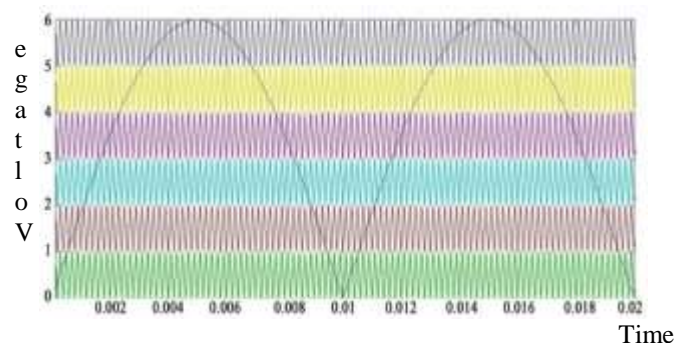


Figure.3 Simulink model of proposed system

A single phase Thirteen level inverter with seven power switches is being analyzed and compared with the existing modified SCML inverter. The operation mode of the topology is analyzed through simulation and its results are given below. The results given below shows that our proposed system works in excellent way and improves the system efficiency and reduce the total harmonic distortion. This paper proposes the power quality problems such as high reactive power and high THD. By using this method the Total harmonics distortion has reduced and thirteen level of output was shown.



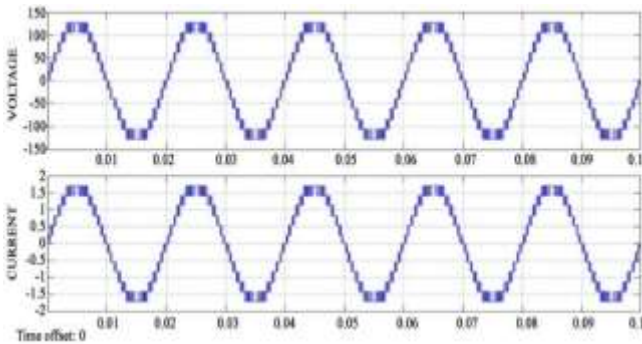


Figure.4 Proposed system Simulink PWM model generation

VI. RESULT

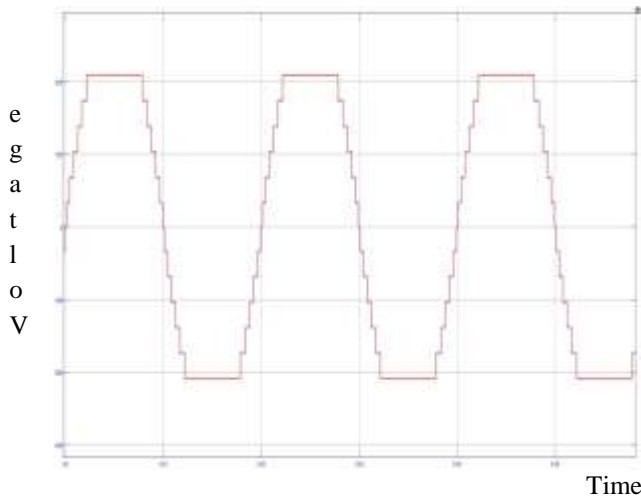


Figure 5. Thirteen level output waveform

The output voltage waveform is showed in the above waveform.

Table 2 :Modulation Index Vs % of THD

S.no	Modulation Index	% of THD
1	0.31	9.18
2	0.79	8.12
3	1	4.02

For this thirteen-level inverter, the MOSFET-based H-bridge was used and three input DC supplies were used. By use of this H-Bridge thirteen level inverter required level output waveform was extracted and successfully verified.

VII. CONCLUSION

It is implemented the study of the modelling and simulation of a 13-level cascaded hybrid multilevel inverter (MLI) with fewer switches. Multilevel inverters produce better output waveforms with less THD. For the suggested multilayer inverter, this study offered a unique PWM switching mechanism. To produce the PWM signals in this paper, just one reference signal is compared to a triangle wave signal. In this multi level inverter, three separate DC voltage levels are utilised. As a result, this setup approach is referred to as asymmetrical cascaded inverter. The suggested architecture of a 13-level cascaded hybrid MLI is supported by satisfactory MATLAB/Simulink model results. This architecture is also mimicked by reducing the most prevalent odd harmonics with the PWM approach. To get a minimal THD value of the load voltage and current, the ratio (1:2:4) of the DC source voltage and the firing angle computation were used. By altering the modulation index between $0 < m < 1$ and keeping the AC output voltage, the realisation of the modulation index is also noticed. It is clear from the foregoing analysis and comparison of output outcomes that the suggested model was successful.

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