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DESIGN OF MODULAR AND NON MODULAR MULTILEVEL INVERTER TOPOLOGY WITH REDUCED NUMBER OF SWITCHES

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ABSTRACT

In this paper, a new multilevel inverter topology with modular and non modular design is developed, which can be operated both symmetrical and asymmetrical mode with a reduced number of power switches. The proposed design has four separated DC sources and Nine active power switches. The topology can be used with symmetrical and asymmetrical voltage source configuration to generate seventeen and seven voltage levels. This structure can be cascaded to produce maximum level by a series connection to produce higher voltage levels with less voltage stress on the switches without modifying the topology structure. Comparison is made with existing topology and recently introduced topologies based on the number of active switches, Separated DC sources, number of gate driver circuits. To prove the presented topology's superiority, a simple Multicarrier pulse width modulation has been deployed as the switching scheme. Validation on the viability of the proposed topology has been carried out through Matlab/Simulink simulation.

KEYWORDS : *Modular, Non Modular Multilevel Inverter, Reduced Switch.*

I. INTRODUCTION

The multilevel inverter (MLI) is basically a voltage source inverter (VSI), which has good ac output voltage wave form in stair case with the rated frequency of 50Hz or 60Hz from single or group of separate dc sources (SDCs) The MLIs is same as the to conventional two level inverters (TLIs) but the MLI can able to produces maximum number of stair case wave form in the output and also has the following merits like lower dv/dt and lesser switching device stress, a minimized output distortion, reduced switching losses, a minimal EMI losses (EMI), the introduction of MLI is emerging last four decades, which is existence in the year 1975, many topologies have been developed by various researchers, which are comprised with many obstacles etc. A new single-phase cascaded multilevel inverter with a series connection in the basic unit and is able to only generate positive levels at the output. The reduction in switching device and driver circuit is added advantage [1]. A new MLI structure called a flexible rung ladder structured multilevel inverter (FRLSMLI), with a savvy to operate both in symmetrical and asymmetrical modes involving only fewer component counts. The FRLSMLI is basically a ladder structured bridge (H-bridge with additional rungs) and the rungs comprise either source inclusion-bypass cell (SIBC) or four level creator cells [2]. A new pulse width modulation strategy is proposed for the multilevel inverter with switching per modulation cycle at each level in MLI which is dependent carrier frequency [3]. A new tapped source stack succored modified HX Bridge MLI topology is developed, which has tapped sources stack (TSS) and modified HX bridge inverter, the systems is implemented with the multicarrier/sub-harmonic pulse width modulation scheme [4]. A new 8-level basic structure for cascaded multilevel inverters is developed with basic structure, two different cascaded multilevel topologies are proposed. The presented cascaded multilevel inverters use less number of power switches, IGBTs and dc voltage sources compared with the conventional

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multilevel inverters [5]. A two-stage switched-capacitor based multilevel inverter has drawback such that switches in the second stage is affected with higher voltage stress. To overcome this problem, a single-stage switched-capacitor module topology for cascaded multilevel inverter is proposed [6]. A non modular matrix structure MLI topology is deployed with reduced switch count. The idea of the modified matrix structure MLI (MMSMLI) is involving switches in columns and separate DC sources (SDCs) in the row links, through which the addition and subtraction amid the SDCs are made easy in the asymmetrical operation, and hence the creation of more output levels are possible [7]. An ingenious symmetrical MLI topology, which consumes lesser component count is proposed with level dependent sources concoction multilevel inverter (LDSCMLI) is basically a multilevel dc link MLI (MLDCMLI), which first synthesizes a stepped dc link voltage using a sources concoction module and then realizes the ac waveform through a conventional H-bridge [8]. Performance analysis of modular and non modular multilevel inverter in various aspects like, topology design, input voltage i.e. symmetric or asymmetric, objectionable components count reduction, modulation index (m), stair case voltage levels, corresponding current wave, Total harmonic distortion (THD) [9]. Asymmetrical multilevel inverter with 1:3 voltage propagation is developed, the Switching pulse for Asymmetrical multilevel inverter are generated using embedded controller with less number of switches and voltage sources compare to conventional multilevel inverters [10]. Modeling of cascaded multilevel inverter (MLI) for harmonics mitigation of induction motor is proposed. Three-phase five- and seven-level inverters are developed with reduced THD [11]. A comparison of sinusoidal and trapezoidal PWM strategies applied to a trinary DC source nine level inverter fed R – load with PI control scheme with sudden load changes at specified reference speed. [12]. A new switching scheme is developed for the cascaded multilevel inverter with PI and FLC controller to produce nine level at the output with lesser THD [13]. A dc to dc converter topology is developed for the solar PV system to harvest the solar energy in efficient manner [14]. A new symmetric multilevel inverter topology is designed with lesser components compared to conventional multilevel inverters [15].

Hence, this study is focused on designing modular and non modular with asymmetric voltage ratio by making a trade-off between, the number of switches, voltage levels, and system structure complexity. In this work, 17-level and 27 level circuit topology is proposed to produce all voltage levels with uniform step size utilizing fewer power switches. The proposed inverter is designed using MATLAB/Simulink software with simulations and verified by experimental results at restive and inductive load. The presented topology is also compared with traditional MLIs and other recently introduced MLIs to show its performance. Its structure and operating principle are addressed in Section II. In section III and IV, the simulation results for modular and non modular design are presented. A comparative study of the proposed inverter against other topologies is carried out in section V. Finally, the conclusion is presented in Section VI.

II. PROPOSED TOPOLOGY

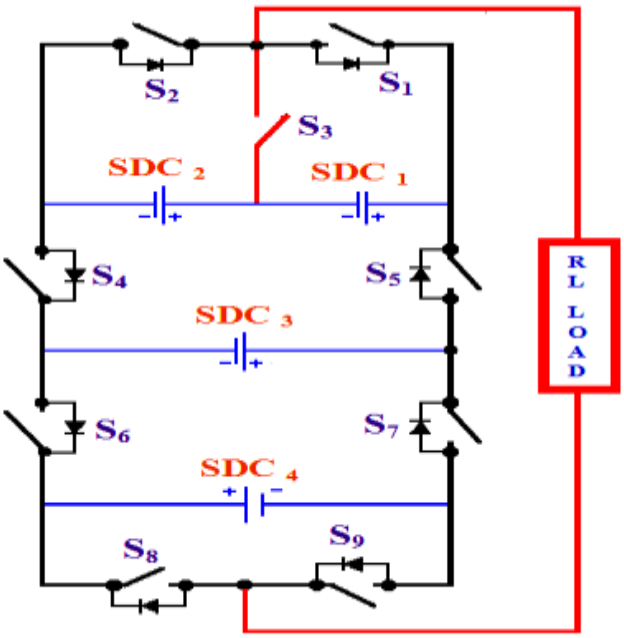

Figure 1: Schematic of Proposed Topology

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The basic skeleton of the proposed inverter circuit is shown in Fig.1. It consists of four separated dc sources (SDCs) with eight unidirectional and one bi-directional power switches. The unidirectional switch is power MOSFET with anti-parallel diode. The bidirectional power switch comprises two power MOSFETs, two anti-parallel diodes, and only one gate-driver circuits. The anti-parallel diodes are used to pass current in both directions, and voltage can be blocked in one direction only. The magnitudes of the SDCs are selected in two aspects. Case 1. For the case of modular the four SDCs are kept as $SDC_1 = SDC_2 = 1$ and $SDC_3 = SDC_4=3$ i.e is 1:1:3:3. Case 2. For the case of non modular the four SDCs are Kept as $SDC_1 = 1$, $SDC_2 = 3$, $SDC_3 = 3$ and $SDC_4 = 3$ i.e is 1:3:3:3. The proposed inverter is suitable for grid tie operation and as well as medium and high power applications. The proposed topology can able to produce 17 voltage level during modular asymmetric configuration can able to generate 17L of 0V, ±1Vdc, ±2Vdc, ±3Vdc, ±4Vdc, v5Vdc, ±6Vdc, ±7Vdc; and ±8Vdc in output with a step size of Vdc. Table 1 tabulates the switching states for proposed 17-level MLI, while Fig. 2 explains the proposed 17-level MLI.

Table 1 shows the switching states of 17-level MLI.

The table 1, shows the switching pattern and the separated dc source voltage, for easy understanding the SDC_1 and SDC_2 are take 1 Volts, and SDC_3 and SDC_4 taken as 3 volts, which can produce a maximum of 17 voltage levels when it is kept under modular and for the non modular it can able to produce 27 voltage levels.

S1	S2	S3	S4	S5	S6	S7	S8	S9	SDC_1	SDC_2	SDC_3	SDC_4	V_0
1	0	0	0	1	0	1	1	0	X	X	X	X	$+8V_{DC}$
0	0	1	0	1	0	1	1	0	X	-	X	X	$+7V_{DC}$
0	1	0	0	1	0	1	1	0	-	-	X	X	$+6V_{DC}$
1	0	0	0	1	0	1	0	1	X	X	X	-	$+5V_{DC}$
0	0	1	0	1	0	1	0	1	X	-	X	-	$+4V_{DC}$
1	0	0	1	0	0	1	1	0	-	-	-	X	$+3V_{DC}$
1	0	0	0	1	1	0	1	0	X	X	-	-	$+2V_{DC}$
0	0	1	0	1	1	0	1	0	X	-	-	-	$+1V_{DC}$
1 0	0 1	0 0	1 0	0 1	0 1	1 0	0 1	1 0	- -	- -	- -	- -	$0V_{DC}$ $0V_{DC}$
0	0	1	1	0	0	1	0	1	-	X	-	-	$-1V_{DC}$
0	1	0	1	0	0	1	0	1	X	X			$-2V_{DC}$
0	1	0	0	1	1	0	0	1	-	-	-	X	$-3V_{DC}$
0	0	1	1	0	1	0	1	0	-	X	X	-	$-4V_{DC}$
0	1	0	1	0	1	0	1	0	X	X	X	-	$-5V_{DC}$
1	0	0	1	0	1	0	0	1	-	-	X	X	$-6V_{DC}$
0	0	1	1	0	1	0	0	1	-	X	X	X	$-7V_{DC}$
0	1	0	1	0	1	0	0	1	X	X	X	X	$-8V_{DC}$

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Table 2. Various parameters for proposed MLI topologies

The table 2, gives the clue to find parameters for proposed MLI topologies.

Parameters	Number of basic units	voltage level
Output Voltage level	16n+1	N_L
Active switches	10n	$5(N_L-1)/8$
Gate drivers	9n	$9(N_L-1)/16$
Power diodes	10n	$5(N_L-1)/8$
Separated dc source	4n	$(N_L-1)/8$

III. MODULAR DESIGN SIMULATION INVESTIGATIONS

For understanding the functioning of the suggested MLI in Modular with asymmetric modes, a detailed simulation study is carried out in MATLAB R2017b. The simulation parameters are as follows, $SDC_1 = SDC_2 = 50$ V and $SDC_3 = SDC_4 = 100$ V i.e. 1:1:2:2 ratio to produce 300 V (peak) in the output voltage. Values of the RL load used in simulation study is R = 100 Ω and L = 100 mH. The switching frequency is 2 kHz. Fig.2 shows 17 level output voltage waveform with modular asymmetric voltage ratio of 1:1:2:2. Fig 3 shows output current waveform with modular asymmetric voltage ratio of 1:1:2:2. Fig. 4 charter output voltage spectra and inductive load current waveform for asymmetrical configuration obtained with 5.62% of THD. The simulation results evidence that the proposed topology is capable of giving high number of voltage levels with a minimum number of power components.

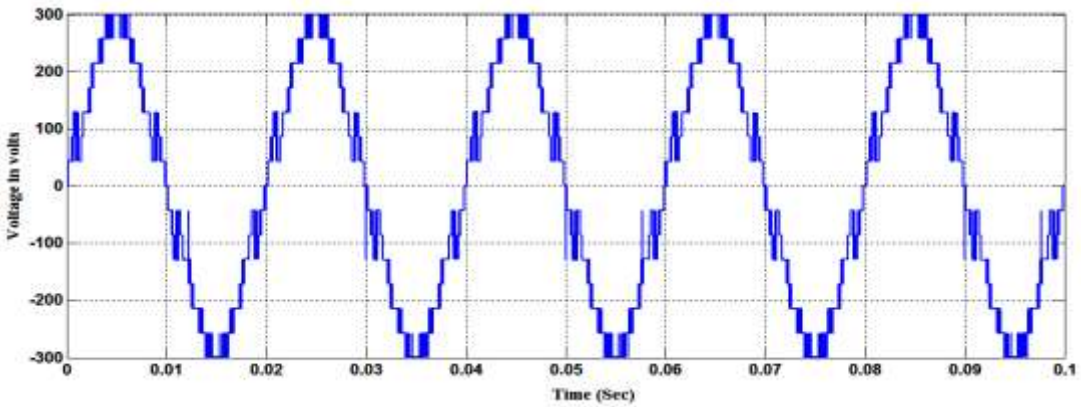

Figure 2: 17 level output voltage waveform with modular asymmetric voltage ratio of 1:1:2:2

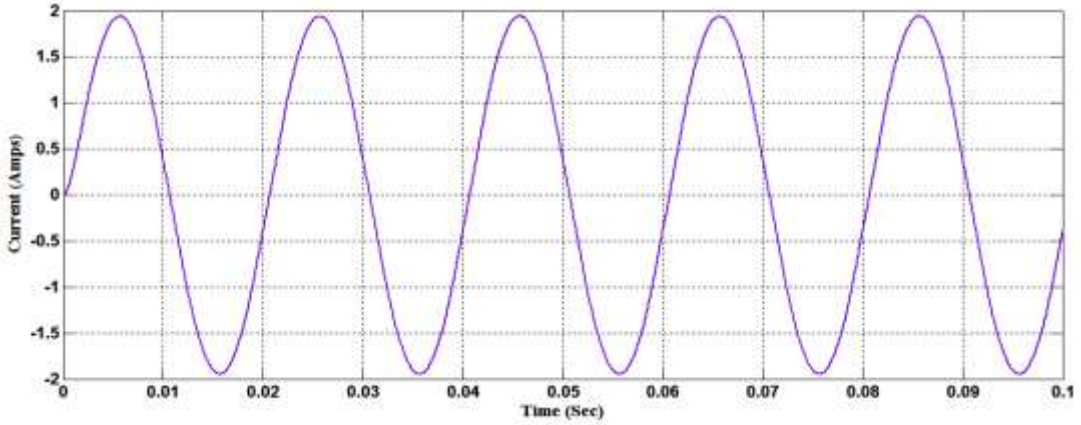

Figure 3: Output current waveform with modular asymmetric voltage ratio of 1:1:2:2

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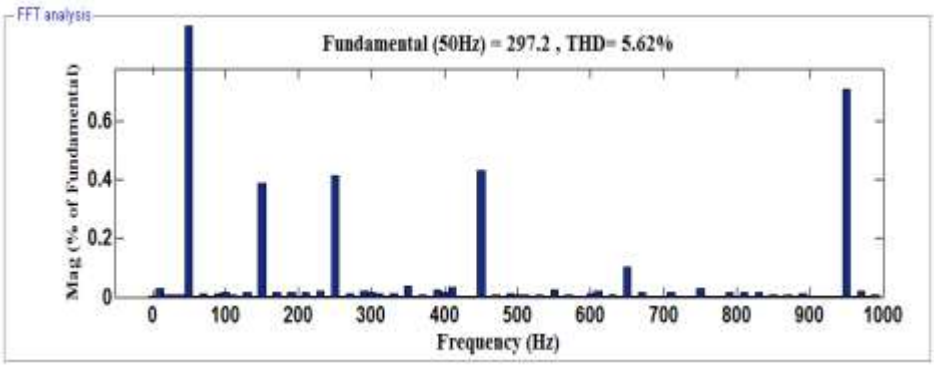

Figure 4: Harmonic spectrum of output voltage asymmetric voltage ratio of 1:1:2:2

IV. NON MODULAR DESIGN SIMULATION INVESTIGATIONS

For understanding the functioning of the suggested MLI in Non Modular with asymmetric modes, a detailed simulation study is carried out in MATLAB R2017b. The simulation parameters are as follows, SDC_1 = 30V, SDC_2= 90 V, SDC_3 = 90 V and SDC_4= 90 V i.e. 1:3:3:3 ratio to produce 300 V (peak) in the output voltage. Values of the RL load used in simulation study is R = 100 Ω and L = 100 mH. The switching frequency is 2 kHz. Fig.5 shows 27 level output voltage waveform with non modular asymmetric voltage ratio of 1:3:3:23. Fig 6 shows output current waveform with non modular asymmetric voltage ratio of 1:3:3:3. Fig. 7 charter output voltage spectra and inductive load current waveform for asymmetrical configuration obtained with 4.01% of THD. The simulation results evidence that the proposed topology is capable of giving high number of voltage levels with a minimum number of power components.

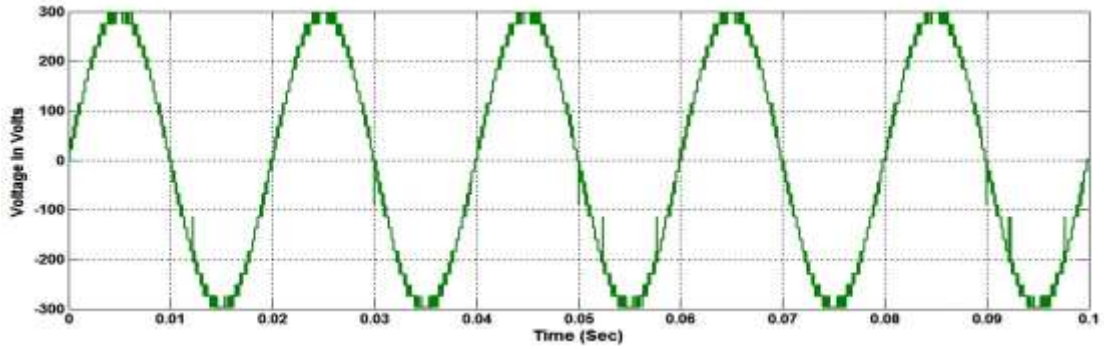

Figure 5: 27 level output voltage waveform with non modular asymmetric voltage ratio of 1:3:3:3

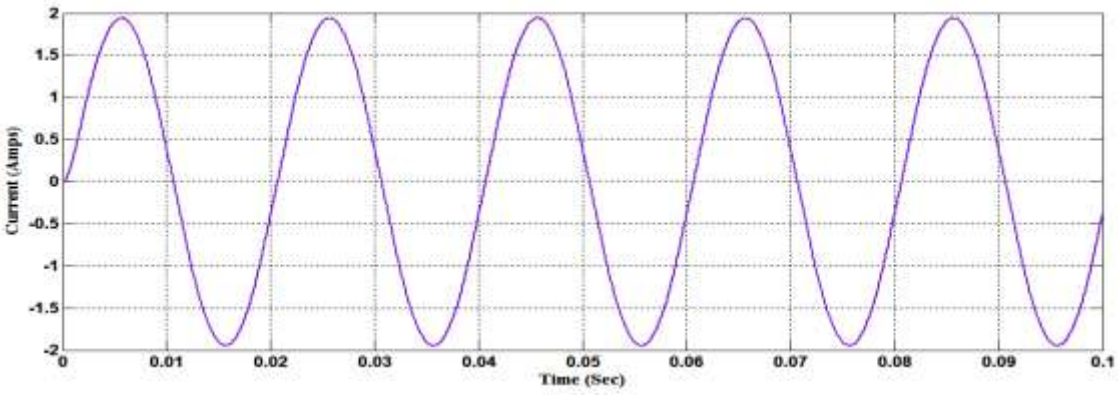

Figure 6: Output current waveform with non modular asymmetric voltage ratio of 1:3:3:3

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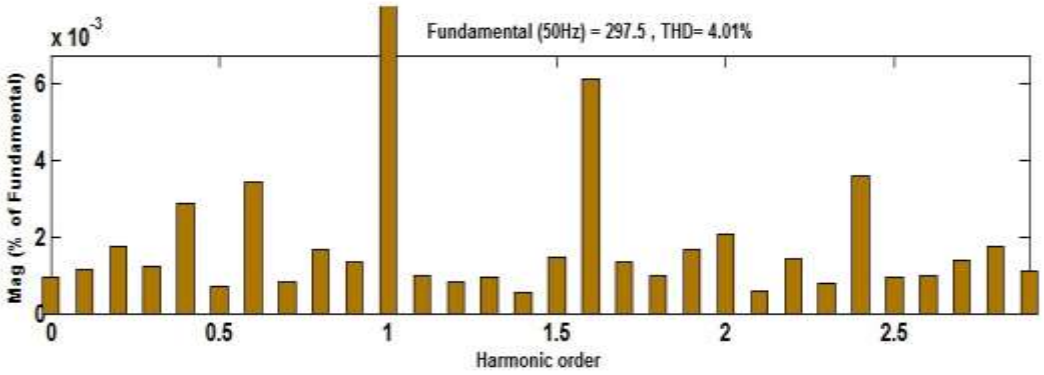

Figure 7: Harmonic spectrum of output voltage asymmetric voltage ratio of 1:3:3:3

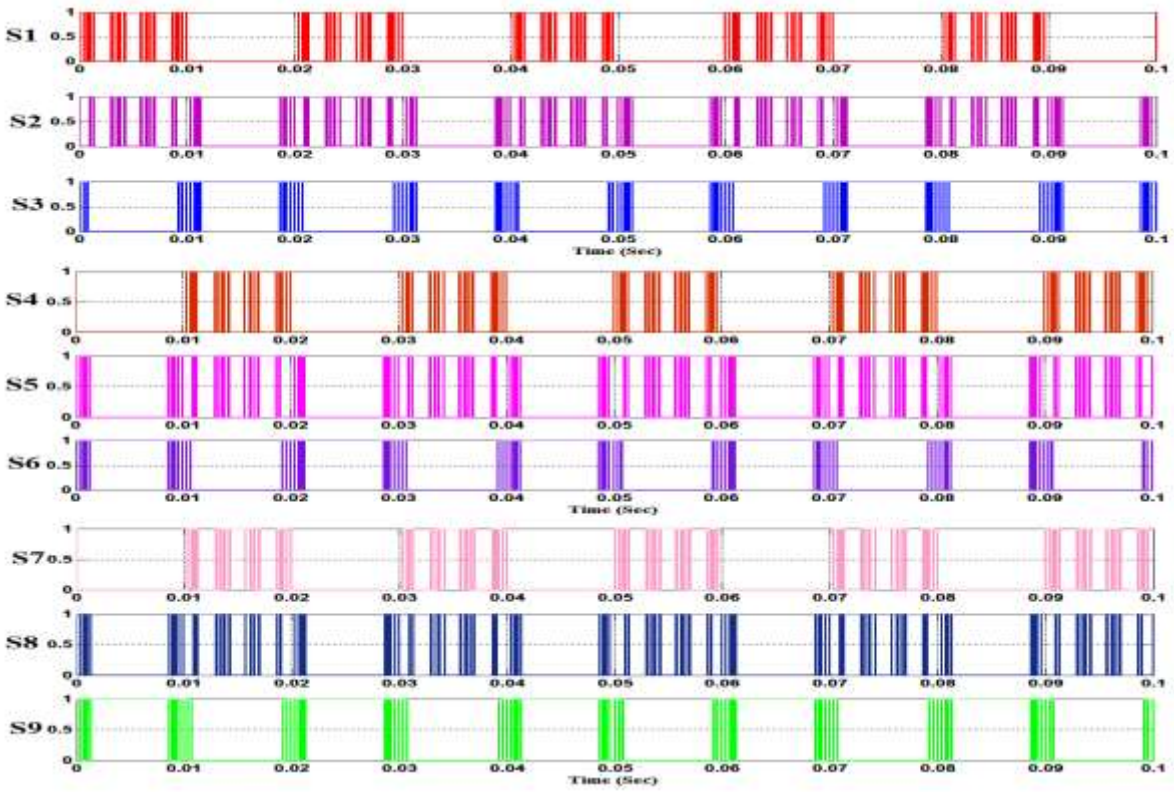

Figure 8: Switching pattern for the MOSFET, S_1 to S_9

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V. COMPARATIVE ANALYSIS WITH PREVAILING TOPOLOGIES

Table 3. Comparison of proposed inverter topology with other topologies

Reference	Switches	Drivers	Diodes	SDCs
Cascaded H B	$2(N_L-1)$	$2(N_L-1)$	$2(N_L-1)$	$(N_L-1)/2$
Flying capacitor	$2(N_L-1)$	$2(N_L-1)$	$2(N_L-1)$	1
NPC	$2(N_L-1)$	$2(N_L-1)$	$2(N_L-1)$	1
2020[2]	$(5N_L+11)/4$	$(5N_L+11)/4$	$(5N_L+11)/4$	3
2020[4]	$(N_L+17/2)$	$(N_L+17/2)$	$(N_L+17/2)$	4
2021[7]	$(5N_L+7)/4$	$(5N_L+7)/4$	$(5N_L+7)/4$	4
Proposed	**$5(N_L-1)/8$**	**$9(N_L-1)/16$**	**$5(N_L-1)/8$**	**4**

V. CONCLUSION

This research work proposed a new single-phase modular and non modular MLI topology. The objective of the proposed MLI is to uses reduced number of power electronics components to produce higher voltage levels with low voltage rated power switches. The topology can generate seventeen voltage levels under modular asymmetric source configuration and twenty seven level under non modular asymmetric source configuration. The inverter topology can be connected in cascade to increase voltage steps with lower power components and lower voltage stress on power components. The proposed inverter's main feature is that it can generate all voltage steps without utilizing an H-bridge inverter. Therefore, it is suitable for medium voltage and high voltage applications. The proposed topology is also compared with traditional MLIs and other recently introduced MLIs in terms of the number of power switches, SDCs, and the number of gate driver's circuits to show its performance. The comparative study shows that this MLI topology uses fewer power switches than other topologies. Simulation results validate the feasibility of the proposed MLI circuit.

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