ISSN (Online): 2455-7838
SJIF Impact Factor (2017): 5.705

EPRA International Journal of

Research & Development

(IJRD)

Monthly Peer Reviewed & Indexed International Online Journal

Volume: 3, Issue:10, October 2018

Published By :
EPRA Journals

SJIF Impact Factor: 5.705 Volume: 3 | Issue: 10 |October| 2018 ISSN: 2455-7838(Online)
EPRA International Journal of Research and Development (IJRD)

POWER AND DELAY ANALYSIS OF ASYNCHRONOUS ADIABATIC ADDERS

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ABSTRACT
Asynchronous adiabatic logic is an attractive approach for low-power design, which combines energy saving benefits of asynchronous systems with adiabatic privileges. In this paper, we have performed power and delay analysis on asynchronous adiabatic full adder circuits. The evaluation is carried out with the intention of reducing power consumption in the full adder circuits. Asynchronous adiabatic design with CMOS logic improves the performance and reduces the power consumption of the circuit. The several asynchronous adiabatic CMOS circuit design styles such as Complementary Pass Transistor with Asynchronous Adiabatic Logic (CPTAAL), Double Pass Transistor with Asynchronous Adiabatic Logic (DPTAAL), and Dual-Rail Domino with Asynchronous Adiabatic Logic (DRDAAL) have been implemented in one-bit full adder circuits, simulated, analyzed, and compared for speed, power consumption, and power-delay product.
KEYWORDS: *Low Power, Asynchronous Adiabatic, Pass Transistor Logic*

1. INTRODUCTION

In recent years, design of low power techniques have firmly expedited the list of VLSI researcher's design interests, in terms of the rising cost of energy, an improving consciousness to green practices, and low power consumption. Moore's law represents the basis of the transistors for VLSI design; it provides the experimental investigation that component density and performance of integrated circuits, doubles every year, which was then reviewed to doubling every two years. Full adder module is the core of several arithmetic operations in microprocessors and Digital Signal Processors. Thus, the design of low power full adder is of great interest. In this paper, we have proposed a unique approach in the full adder design, asynchronous adiabatic logic with CMOS circuit design styles, has been followed to obtain the energy saving gains with improved circuit performance. From the literature, we found that, Complementary Pass-Transistor Logic (CPL) circuits consume less power than conventional static circuits because the logic swing of the pass transistor outputs is smaller than the supply voltage level. In Double Pass-Transistor Logic circuits, full swing operation is accomplished by simply adding PMOS transistors in parallel with the NMOS transistors. Thus, the problems of noise margin and speed degradation at reduced supply voltages associated in CPL circuits are avoided.

Dual-Rail Domino Logic (DRDL) is a precharge circuit technique which is used to improve the speed of CMOS circuits. Asynchronous adiabatic logic (AAL) is combined with these three CMOS logic styles to obtain the energy saving benefits with improved circuit performance and reduced power consumption in full adder design. In this paper, asynchronous adiabatic CMOS circuit design styles such as Complementary Pass Transistor with Asynchronous Adiabatic Logic (CPTAAL), Double Pass Transistor with Asynchronous Adiabatic Logic (DPTAAL), and Dual-Rail Domino with Asynchronous Adiabatic Logic (DRDAAL) are reported and discussed in further sections. The most significant parameters are considered for analysis such as power consumption, delay and power-delay product to measure the quality of the proposed circuit and to compare various circuit styles [1].

2. ADIABATIC LOGIC DESIGN

"Adiabatic" relates to a system in which a transition occurs without energy (usually in the form of heat) being either lost to or gained from the system. In the context of use of electronic systems, electronic charge is preserved rather than heat. By moving to a computing model that is reversible, energy can be reprocessed from a computing engine, and reused to perform further calculations. This style of logical approach differs from CMOS circuits, which dissipate energy during switching. To reduce the dynamic power, there are some conventional approaches such as reducing supply voltage, decreasing physical capacitance and reducing switching activity. These approaches are not conforming enough to meet today's power requirement. Adiabatic system operates with the concept of switching activities, which reduces the power by providing stored energy back to the supply. In the adiabatic techniques, the main design changes are focused in power clock, which plays the essential role in the principle of operation. The following major design rules for the adiabatic circuit design are accomplished in each phase of the power clock.

1. Never turn on a transistor if voltage exists across it (VDS>0)
2. Never turn off a transistor if current exists across it (IDS≠ 0)
3. Never pass current through a diode

In all the four phases of power clock, if these requirements are met, recovery phase will restore the energy to the power clock, resulting significant energy saving. Despite some complexities in adiabatic logic design perpetuate. Two such complexities are circuit implementation for time-varying power sources needs to be done, and computational implementation by low overhead circuit structures, needs to be followed [2]

3. ASYNCHRONOUS ADIABATIC LOGIC (AAL)

Asynchronous Adiabatic Logic is a unique design technique which combines the energy saving benefits of asynchronous logic and adiabatic logic. Like adiabatic circuits, asynchronous adiabatic circuits are also a promising technology for low-power, highly modular digital circuits. AAL eliminates the need of power clock generators, also overcomes the problems associated with the generation and routing of the clocks in adiabatic systems. Another benefit of AAL is the fact that, when an asynchronous system is idle, it will not utilize clock signals, whereas, in synchronous adiabatic systems, these clock signals are propagated throughout the entire system and will convert energy to heat, often without performing any useful computations. In contrast to the synchronous adiabatic circuits, asynchronous adiabatic circuits perform handshaking between their components, to perform all necessary synchronization, communication, and sequencing of operations. The main privilege of this circuit is its low power consumption, stemming from its elimination of clock drivers and the fact that no transistor ever transitions unless it's performing a useful computation [3].

3.1 Proposed Design

The main objective of this paper is to design low power full adder using asynchronous adiabatic technique with pass transistor logic. The logic scheme for the proposed full adder cell is illustrated in Fig.1. In this, entire system consists of two main blocks, such as logical block and control and regeneration (C&R) block. As in Fig.1, data output signal of any adiabatic logical block is not only going into next logical block as data input, but at the same time, it is used to generate a control signal for the next logical block using C&R block. This technique helps to save the required power clock generator with less power than any other designs.

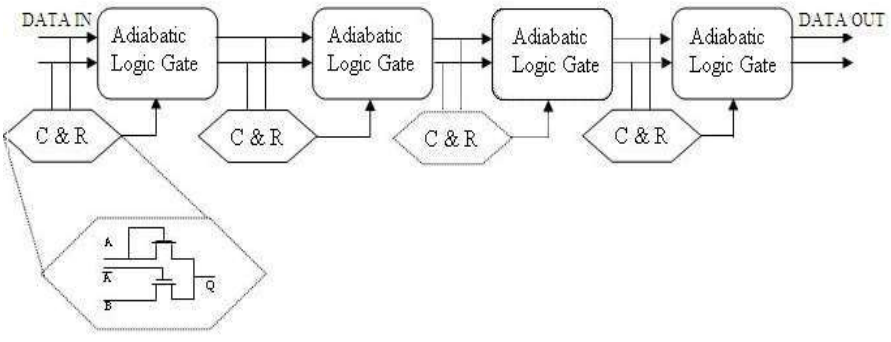

Fig. 1. Logic scheme for the proposed full-adder

3.2 Control and Regeneration (C&R) Block

The control and regeneration (C&R) block is given in Fig.2. In the proposed design, asynchronous operation has been achieved by the control and regeneration part. C&R block generates the control signal for the next logical stage with the help of the previous stage output signal. The regeneration technique makes the control signal strong enough to drive the next logical block.

The local regeneration stores the intermediate energy. This energy is provided to the required

operations for the next level of logic. This C&R block controls and regenerates the energy required for the next operation to the next logical block.

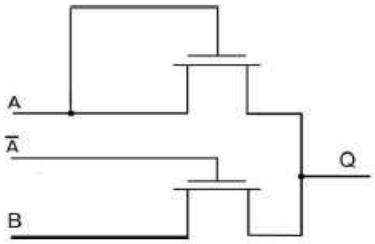

Fig. 2. Control and Regeneration (C&R) block

The pass transistor logic implementation is used for the design of C&R block in terms of energy efficiency and functionality. The simple construction of the pass transistor logic makes it simple to adjust the sizing of transistors to get the desired charging and discharging time; hence the slope of the output control signal minimizes the power. The inputs of this C&R blocks are A, A bar and B, fed from the output of adiabatic logic gates. In this, NOR portion of the OR gate is serving as the control part whereas the NOT portion is not only making the desired logical inversion. At the same time, it performs the regeneration of the signal. The regenerated signal energy will be used in the next logic circuit for the sequential operation. The NOT portion will again regenerate the signal whereas the operation gets completed. In this way, the output signal 'Q' of this C&R blocks promotes the local storage of energy and will switch the circuit for recovery. Control block is also used to follow and preserve the power clock sequences with the input vectors. Regeneration gives power saving strategy. All logic gates or logic sequences are connected through C&R structure. The throughput of the logical systems is reduced by the intermediate C&R blocks due to the asynchronous mode of operation. The system energy will be circulating among the logical circuits, and the minimum power is required from the power clock generator for the operation. Generally, the regenerated signal is stored and circulated between the C&R and logical part. Thus, there will not be much power reverse to the power clock system. It helps to reduce the power clock system switching losses [3].

3.3 CPTAAL Full Adder

The schematic diagram of the CPTAAL full adder circuit is shown in Fig. 3. In this, asynchronous adiabatic full adder logic uses complementary pass-transistor logical block with C&R structures. It has been designed and tested to get the best power efficiency out of the proposed system.

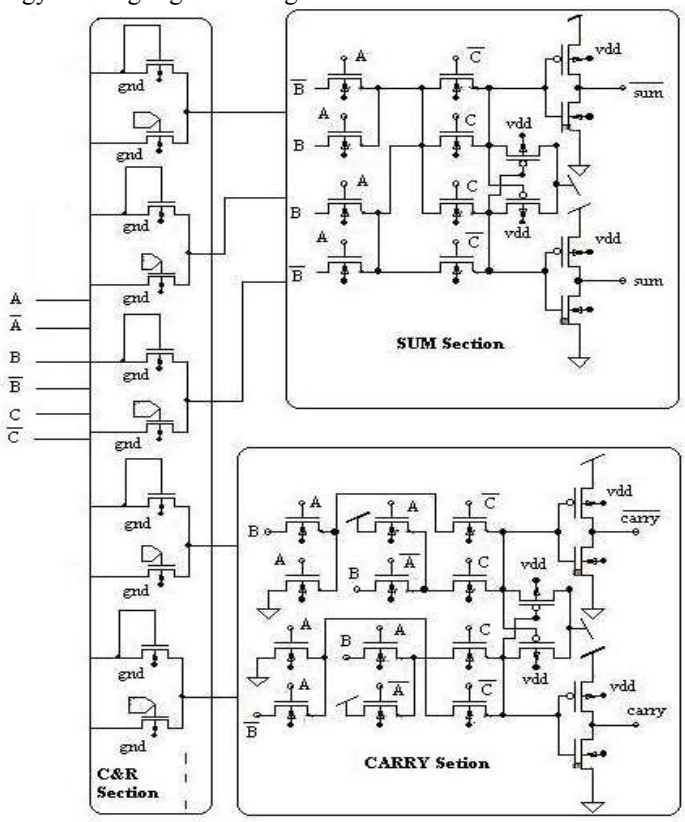

Fig.3. CPTAAL full adder

The main difference of pass-transistor logic design compared to the CMOS logic design is that the source side of the logic transistor networks is connected to some input signals instead of the power lines. The benefit is that one pass-transistor network (either NMOS or PMOS) is sufficient to perform the logic operation, which results in a smaller number of transistors and smaller input loads, especially when NMOS networks are used. The proposed CPTAAL design uses only an NMOS network for the implementation of logic functions and has differential inputs and outputs, thus resulting in low input capacitance, good output driving capability and high-speed operation. As the high voltage level of the pass-transistor outputs is lower than the supply voltage level by the threshold voltage of the pass transistors, the signals have to be amplified by using CMOS inverters at the outputs. A simple implementation of the proposed system is depicted. It is a full adder, with the logical part designed using asynchronous adiabatic logic, and whereas the control part of the C&R block and regeneration part is made of pass-transistor logic. This series pass transistor logic is functioning as transmission gate in the output logic of each gate structure [4].

3.4 DPTAAL Full Adder

The DPTAAL design of full adder cell is presented in Fig.4, which consists of C&R section, adiabatic DPL full adder circuit, multiplexer section, and an output buffer. In this DPTAAL full adder, sum circuit section includes DPL XOR gate, a DPL multiplexer, C&R section, and an output buffer. The carry output section consists of DPL AND gate, DPL OR gate, a DPL multiplexer, C&R section, and an output buffer. These adiabatic DPL gates consists NMOS and PMOS pass transistors to achieve full swing operation. When the inputs A, B, and C are all low, the outputs SUM bar and CARRY bar will be acting as the current paths. Thus, two current paths for each output can be achieved. In this DPTAAL design, power and clock lines are mixed into a single power clock line which has both functions of powering and timing the circuit. C&R section is the main concept of this DPTAAL design, which generates the control signal for the next logical gate using the output signal of the previous gate. The regeneration technique makes the control signal strong enough to drive the next logical gate. Thus, power consumption from the power clock is reduced drastically. A multiplexer chooses the output to be one of several inputs based on a select signal. In this full adder design, DPL multiplexer (Fig.5) is used to select the required outputs of DPL-XOR, DPL-OR, and DPL- AND, based on the inputs C and C bar. The schematic diagrams of these DPL logical gates are shown in Fig.6, 7, 8. All these full adder blocks have been designed with PMOS/NMOS transistors, focusing on low power consumption and high efficient operation [5].

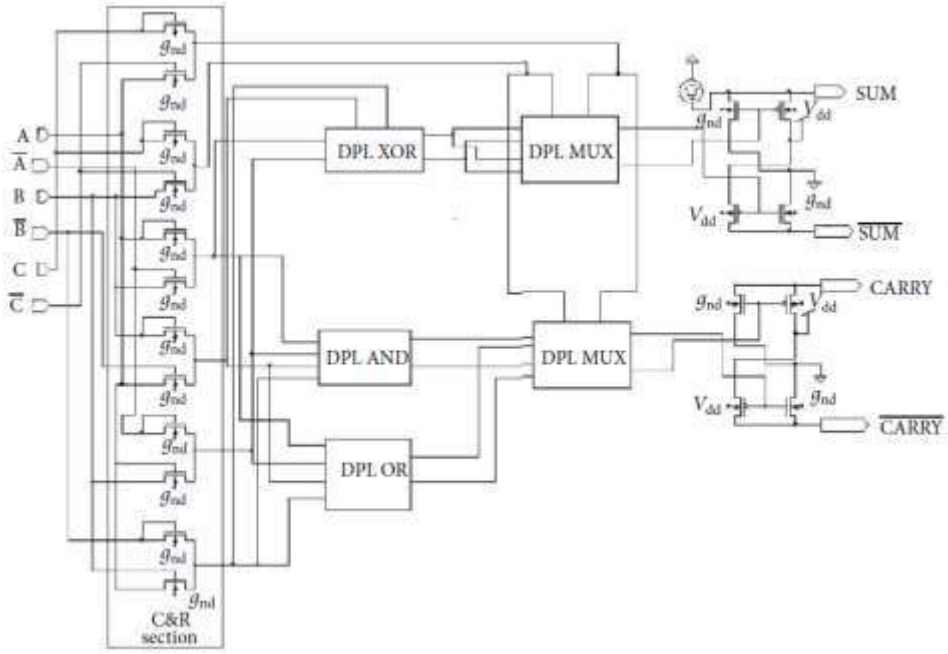

Fig.4. DPTAAL full adder

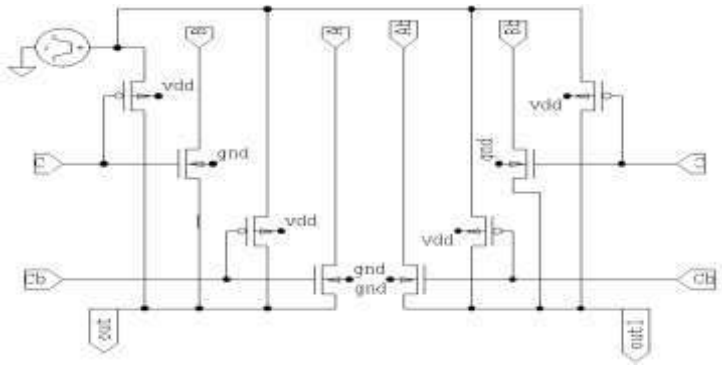

Fig.5. DPL MUX schematic

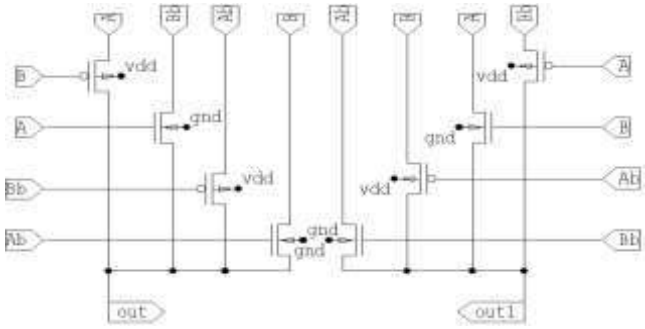

Fig.6. DPL XOR schematic

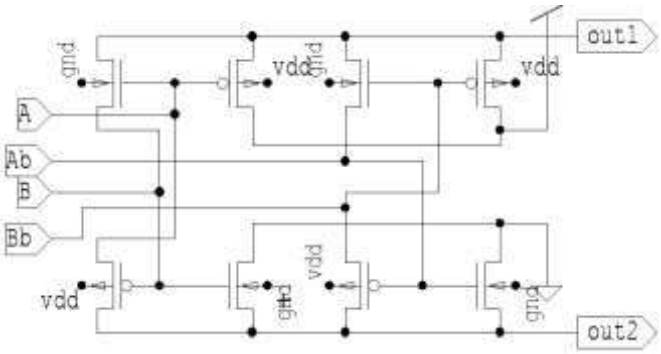

Fig.7. DPL OR schematic

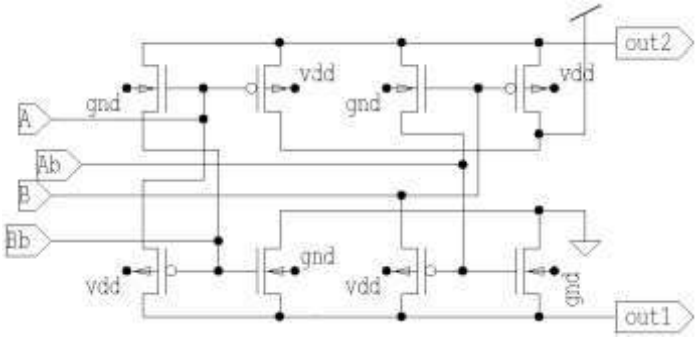

Fig.8. DPL AND schematic

3.5 DRDAAL Full Adder

Dual-Rail Domino Logic (DRDL) is a precharged technique which is used to improve the speed of CMOS circuits. It exhibits a low delay; it is usually used in high-performance circuits. It is based on an NMOS pull-down network and a PMOS pair, driven by the clock, which brings the gate in the precharge or evaluation mode. The output-inverters assure that no race occur while the weak feedback PMOS transistors allow to reduce the charge-redistribution problem, increasing the noise immunity. A unique approach,

DRDL with asynchronous adiabatic technique (DRDAAL), has been followed in the full adder design. Asynchronous adiabatic full adder design uses dual-rail domino logical blocks with C&R

structures. It has been designed and tested to get the power efficiency. A simple implementation of the proposed system is depicted in the Fig. 9. A domino gate consists of a dynamic CMOS circuit followed by a static CMOS buffer. In this DRDAAL design, asynchronous operation has been achieved by the control and regeneration (C&R) section, which generates the control signal for the next logical gate using the output signal of the previous gate. The dynamic circuit consists of a PMOS precharge transistor and an NMOS evaluation transistor with the clock signal applied to their gate nodes, and an NMOS logic block which implements the required logic function. During the precharge phase, the output node of the dynamic circuit is charged through the precharged PMOS transistor to the supply voltage level.

The output of the static buffer is discharged to ground. During the evaluation phase, the evaluation NMOS transistor is ON, and depending on the logic performed by the NMOS logic block, the output of the dynamic circuit is discharged, or it will stay precharged. The major scope of the dynamic, precharged design styles over the static styles is that they eliminate the spurious transitions and the corresponding power dissipation.

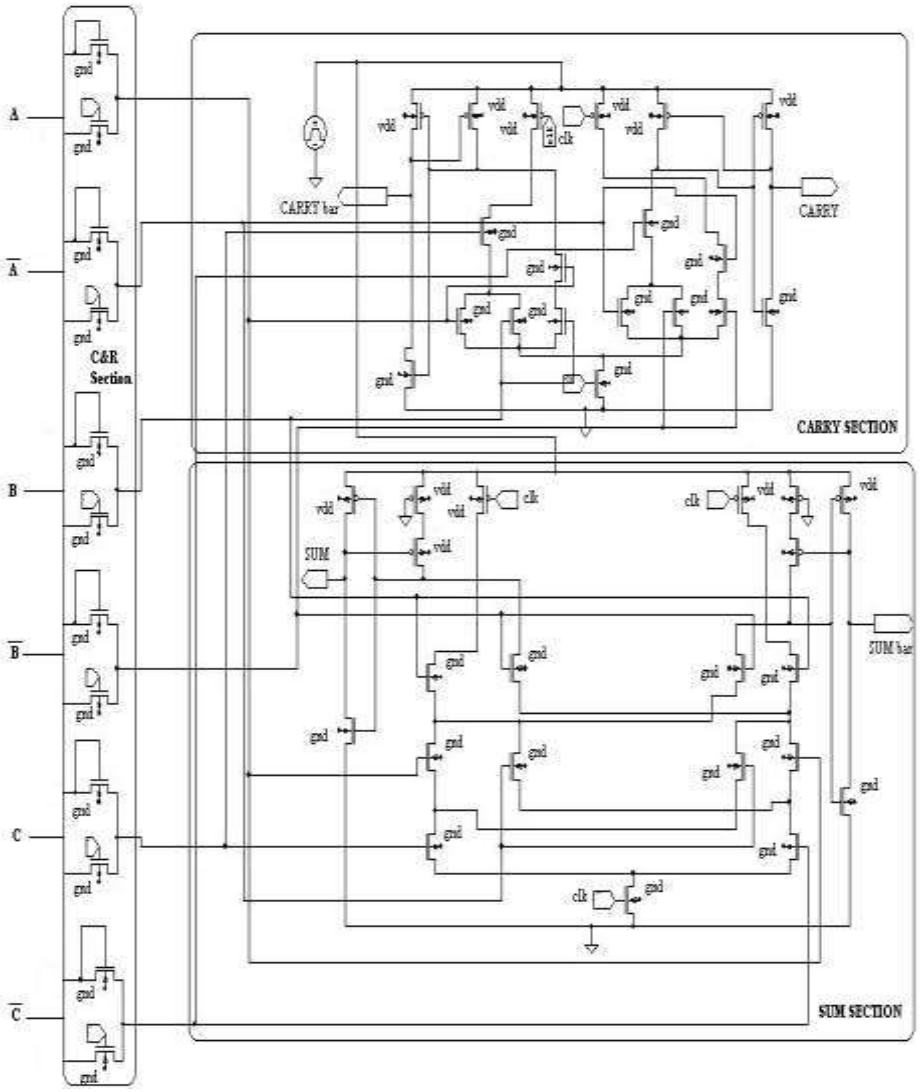

Fig. 9. DRDAAL full adder cell.

4. RESULTS AND DISCUSSION

Asynchronous adiabatic design of full adder using various CMOS logic has been implemented. CMOS logic is introduced to improve speed performance in the circuits. It also exhibits a low delay. For the various frequency ranges, the average power consumed, delay of the circuit, and power-delay product (PDP) of the proposed full adders are compared with the conventional CMOS full adder and the synchronous adiabatic full adder designs namely, Positive feedback adiabatic logic (PFAL) adder, Transmission gate based adiabatic logic (TGAL) adder, reported in Table 1.Compared with the conventional CMOS implementation and the synchronous adiabatic adder designs, the proposed asynchronous adiabatic adders achieve power savings of 15 to 85% for clock rates ranging from 100 to 200MHz. In the proposed designs, the transistor count of the DPTAAL full adder is

increased as compared with CPTAAL and DRDAAL designs; hence a large on-chip area overhead is associated with DPTAAL design. Taking into consideration the gain in energy efficiency and performance, the area overhead is acceptable.

Table I. Power consumption, Delay and PDP Performances of full adder designs

Logic Design	Performance Metrics	Frequency (MHz)			
		1	10	100	200
CPTAAL	Power (μW)	0.074	0.096	0.147	0.206
	Delay (ns)	54	51	48	45
	Power Delay Product (fJ)	4	4.9	7.1	9.3
DPTAAL	Power (μW)	0.116	0.135	0.197	0.342
	Delay (ns)	43	40	38	35
	Power Delay Product (fJ)	5	5.4	7.5	12
DRDAAL	Power (μW)	0.182	0.222	0.265	0.550
	Delay (ns)	34	31	29	24
	Power Delay Product (fJ)	6.2	6.9	7.7	13.2
PFAL	Power (μW)	0.21	0.25	0.5	3.2
	Delay (ns)	35	31	28	23
	Power Delay Product (fJ)	7.35	7.75	14	74
TGAL	Power (μW)	0.35	0.7	1.3	3.65
	Delay (ns)	46	41	38	20.05
	Power Delay Product (fJ)	16	29	49	73
Conventional CMOS	Power (μW)	0.7	1.12	2.95	7.54
	Delay (ns)	107	67	25	10
	Power Delay Product (fJ)	75	75	75	75

The transistor counts of the proposed full adders are compared with conventional CMOS and adiabatic full adders, given in Table 2. The power, delay and PDP comparison graph for the proposed asynchronous adiabatic adders are shown in the Fig.10, 11and 12.

Table II. Transistor Count Comparison of full adder designs

Logic Design	No. of Transistors
CPTAAL	56
DPTAAL	65
DRDAAL	52
PFAL	38
TGAL	60
Conventional CMOS	28

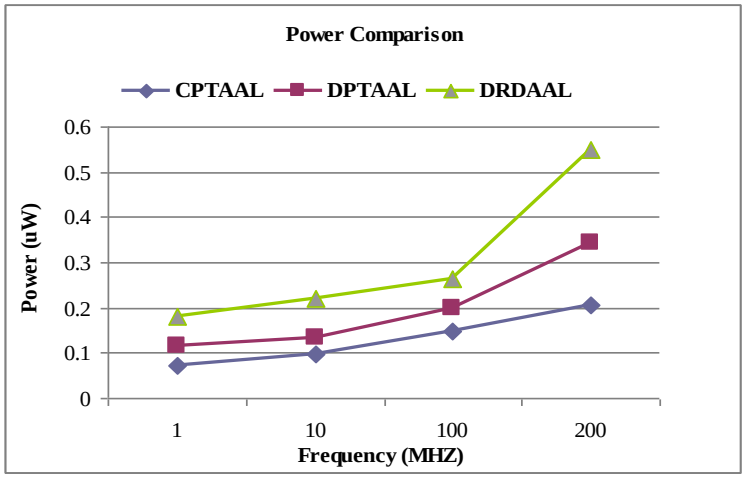

Fig.10. Power Comparison graph for the proposed adders

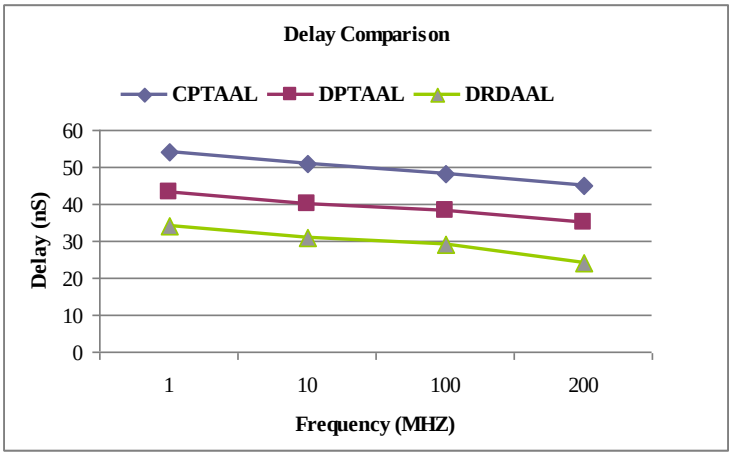

Fig. 11. Delay Comparison graph for the proposed adders

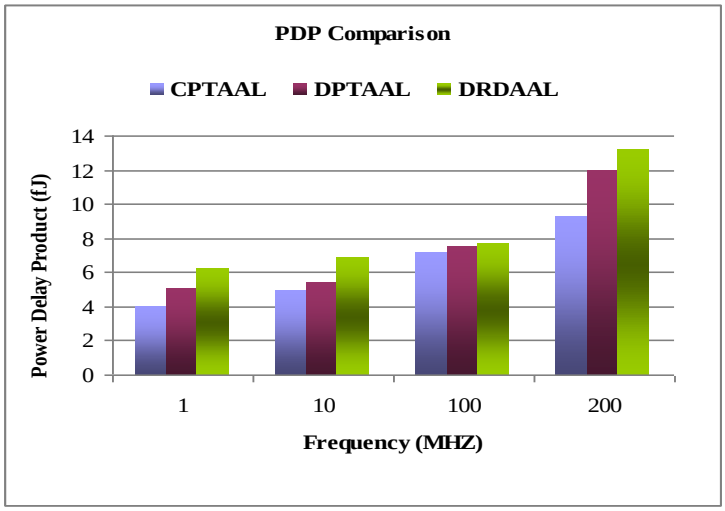

Fig. 12. Power Delay Product Comparison graph for the proposed adders

5. CONCLUSIONS

In this paper, we have performed power and delay analysis of asynchronous adiabatic full adders using CPTAAL, DPTAAL and DRDAAL techniques. The power, delay and PDP performances of these designs are compared. The CPTAAL approach offers less power consumption in the full adder circuit than the other design. It is suitable for complex arithmetic circuits where no compromise on power dissipation is allowed. The DPTAAL approach offers a more reasonable trade-off between power and delay in the full adder circuit. These circuits can be used to improve the circuit performance at reduced voltage level. The DRDAAL approach exhibits the lowest delay in the full adder

circuit, having a power dissipation penalty greater than the speed improvement. It is suitable for complex arithmetic circuits where no compromise on performance is allowed. The proposed full adder circuits have been implemented and studied using 0.18µm TSMC technology file with 1.8V supply voltage and have shown great prospect for the development of power aware systems. Further, these designs can be extended to multiplier, and multiplier-accumulator circuits to validate the feasibility of asynchronous adiabatic circuits in low power computing applications.

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