



## DESIGN OF LOW-POWER HIGH-PERFORMANCE 2–4 AND 4–16 MIXED-LOGIC LINE DECODERS

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### ABSTRACT

*The invention of integrated circuits there has been a continuous demand for high performance, low power and low area or low cost diversified application from a variety of consumers. This demand has been pushing the fabrication process sub micron technologies such as 32, 22, 14nm and so on. The various technology aspects for low power applications are reviewed in detail, along with the evaluation of new technology, bearing in mind the power, performance and area. We are going to design 2-4 and 4-16 decoders with mixed logic design. Mixed logic is a gate-level design. It allows a digital logic circuit designer to separate the functional description of the circuit from its physical implementation. The use of mixed logic design provides logic expressions and logic diagrams that are analog of each other. In order to design these decoders there are two topologies are presented for the 2–4 decoder: a 14-transistor topology aiming on minimizing transistor count and power dissipation and 15-transistor topology aiming on high power-delay performance. Both normal and inverting decoders are implemented in each case, yielding a total of four new designs. Furthermore, four new 4–16 decoders will be designed by using mixed-logic 2–4 pre-decoders combined with standard CMOS post-decoder. All proposed decoders have full-swinging capability and reduced transistor count compared to their conventional CMOS counterparts. Finally, a variety of comparative spice simulations at some area by using these comparative simulations we can show that the proposed circuits present a significant improvement in power and delay, outperforming CMOS in almost all cases.*

**INDEX TERMS**—Line decoder, mixed-logic, power-delay optimization.

### I. INTRODUCTION

Very large scale integration (VLSI) is the process of creating an integrated circuit (IC) by combining thousands of transistors into a single chip. Over the past decade, power consumption of VLSI chips has constantly been increasing. Moore's Law drives VLSI technology to continuous increases in transistor densities and higher clock frequencies. The trends in VLSI technology scaling in the last few years show that the number of on-chip transistors increase about 40% every year. The operating frequency of VLSI systems increases about 30% every year. Although capacitances and supply voltages scale down meanwhile, power consumption of the VLSI chips is increasing continuously. On the other hand, cooling systems cannot improve as fast as the power consumption

increases. Therefore in the very close future chips are expected to have limitations of cooling system and solving this problem will be expensive and inefficient.

The main objective of Analysis of low power high performance 2-4 and 4-16 mixed line logic decoders is to reduce the power consumption. The power consumption can be reduced by minimizing the transistor count by using mixed logic design when compared to CMOS logic design. We design 2-4 and 4-16 decoders using mixed logic as well as CMOS logic and compare the results between them. In VLSI systems there is a trade-off between three parameters those are power, area and speed. To obtain better results in two parameters the third parameter should be negligible. Here we are designing low power and high performance decoders

individually. So in order to design a low power and area efficient decoder speed has less preference. In order to design high performance and area efficient decoder power has less preference.

Line decoders are fundamental circuits, widely used in the peripheral circuitry of memory arrays.

**II. OVERVIEW OF LINE DECODER CIRCUITS**

In digital systems, discrete quantities of information are represented by binary codes. An  $n$ -bit binary code can represent up to  $2^n$  distinct elements of coded data. A decoder is a combinational circuit that converts binary information from  $n$  input lines to a maximum of  $2^n$  unique output lines or fewer if the  $n$ -bit coded information has unused combinations. The circuits examined here are  $n$ -to- $m$  line decoders, which generate the  $m = 2^n$  min terms of  $n$  input variables.

**A. 2-4 Line Decoder**

A 2-4 line decoder generates the 4 min terms  $D_0-D_3$  of 2 input variables  $A$  and  $B$ . Its logic operation is summarized in Table I. Depending on the input combination; one of the 4 outputs is selected and set to 1, while the others are set to 0. An inverting 2-4 decoder generates the complementary min terms  $I_0-I_3$ , thus the selected output is set to 0 and the rest are set to 1, as shown in Table II. In conventional CMOS design, NAND and NOR gates are preferred to AND and OR, since they can be implemented with 4 transistors, as opposed to 6, therefore implementing logic functions with higher efficiency. A 2-4 decoder can be implemented with 2 inverters and 4 NOR gates Fig. 1(a), whereas an inverting decoder requires 2 inverters and 4 NAND gates Fig. 1(b), both yielding 20 transistors

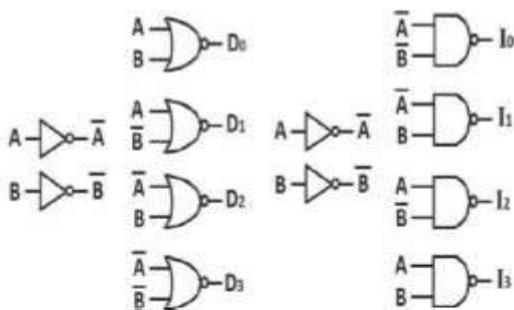


Figure 1: a) Non Inverting NOR based Decoder. b) Inverter NAND based decoder

Table 1: Truth Table of 2-4 decoder

A	B	D0	D1	D2	D3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Table 2: Truth Table of Inverting 2-4 decoder

A	B	I0	I1	I2	I3
0	0	0	1	1	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	1	1	1	0

**B. 4-16 Line Decoder With 2-4 Pre decoders**

A 4-16 line decoder generates the 16 min terms  $D_0-15$  of 4 input variables  $A, B, C,$  and  $D$ , and an inverting 4-16 line decoder generates the complementary min terms  $I_0-15$ . Such circuits can be implemented using a pre-decoding technique, according to which blocks of  $n$  address bits can be pre-decoded into 1-of- $2^n$  pre-decoded lines that serve as inputs to the final stage decoder [1]. Therefore, a 4-16 decoder can be implemented with 2 2-4 inverting decoders and 16 2-input NOR gates [Fig. 2(a)], and an inverting one can be implemented with 2 2-4 decoders and 16 2-input NAND gates [Fig. 2(b)]. In CMOS logic, these designs require 8 inverters and 24 2-input gates, yielding a total of 104 transistors each.

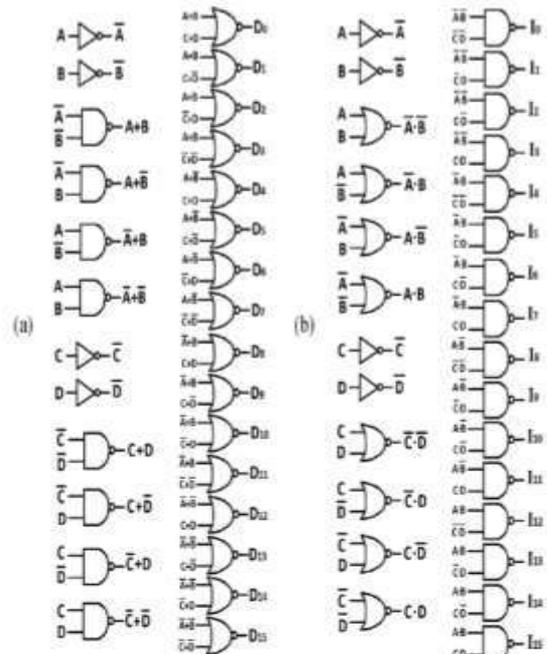


Figure 2: Non inverting and inverting decoders using 2-4 pre decoders and post decoders

**III. NEW MIXED-LOGIC DESIGNS**

Transmission gate logic (TGL) can efficiently implement AND/OR gates [5], thus it can be applied in line decoders. The 2-input TGL AND/OR gates are shown in Fig. 3(a) and (b), respectively. They are full-swinging, but not restoring for all input combinations. Regarding PTL, there are two main circuit styles: those that use nMOS-only pass transistor circuits, like CPL [3], and those that use both nMOS and pMOS pass transistors, like DPL [4]

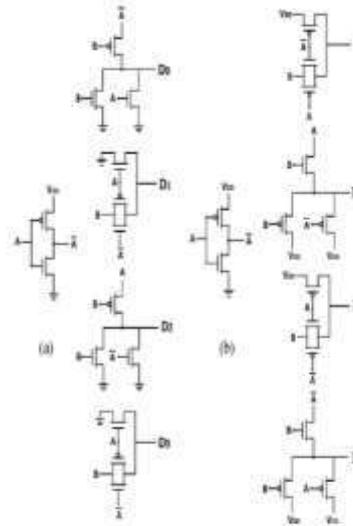
and DVL [6]. The style we consider in this work is DVL, which preserves the full swing operation of DPL with reduced transistor count [10]. The 2-input DVL AND/OR gates are shown in Fig. 3(c) and (d), respectively. They are full- swinging but non-restoring, as well. Assuming that complementary inputs are available, the TGL/DVL gates require only 3 transistors. Decoders are high fan-out circuits, where few inverters can be used by multiple gates, thus using TGL and DVL can result to reduced transistor count. An important common characteristic of these gates is their asymmetric nature, ie the fact that they do not have balanced input loads. As shown in Fig. 3, we labeled the 2 gate inputs  $X$  and  $Y$ . In TGL gates, input  $X$  controls the gate terminals of all 3 transistors, while input  $Y$  propagates to the output node through the transmission gate. In DVL gates, input  $X$  controls 2 transistor gate terminals, while input  $Y$  controls 1 gate terminal and propagates through a pass transistor to the output. We will refer to  $X$  and  $Y$  as the control signal and propagate signal of the gate, respectively. Using a complementary input as the propagate signal is not a good practice, since the inverter added to the propagation path increases delay significantly. Therefore, when implementing the inhibition ( $A\bar{B}$ ) or implication ( $A\bar{B} + B$ ) function, it is more efficient to choose the inverted variable as control signal. When implementing the AND ( $AB$ ) or OR ( $A + B$ ) function, either choice is equally efficient. Finally, when implementing the NAND ( $\overline{A\bar{B}}$ ) or NOR ( $\overline{A+B}$ ) function, either choice results to a complementary propagate signal, perforce.

**A. 14-Transistor 2-4 Low-Power Topology**

Designing a 2-4 line decoder with either TGL or DVL gates would require a total of 16 transistors (12 for AND/OR gates and 4 for inverters). However, by mixing both AND gate types into the same topology and using proper signal arrangement, it is possible to eliminate one of the two inverters, therefore reducing the total transistor count to 14.

Let us assume that, out of the two inputs, namely,  $A$  and  $B$ , we aim to eliminate the  $B$  inverter from the circuit. The  $D_0$  minterm ( $\overline{A\bar{B}}$ ) is implemented with a DVL gate, where  $A$  is used as the propagate signal. The  $D_1$  minterm ( $AB$ ) is implemented with a TGL gate, where  $B$  is used as the propagate signal. The  $D_2$  minterm ( $\overline{A\bar{B}}$ ) is implemented with a DVL gate, where  $A$  is used as the propagate signal. Finally, The  $D_3$  minterm ( $AB$ ) is implemented with a TGL gate, where  $B$  is used as the propagate signal. These particular choices completely avert the use of the complementary  $B$  signal; therefore, the  $B$  inverter can be eliminated from the circuit, resulting in a 14-transistor topology (9 nMOS and 5 pMOS). Following a similar procedure with OR gates, a 2-4 inverting line decoder can be implemented with 14 transistors (5 nMOS and 9 pMOS) as well:  $I_0$  and  $I_2$  are implemented with TGL (using  $B$  as the

propagate signal), and  $I_1$  and  $I_3$  are implemented with DVL (using  $A$  as the propagate signal). The  $B$  inverter can once again be elided. Inverter elimination reduces the transistor count, logical effort and overall switching activity of the circuits, thereby reducing power dissipation. The two new topologies are named “2-4LP” and “2-4LPI,” where “LP” stands for “low power” and “I” for “inverting.” Their schematics are shown in Fig. 4(a) and (b), respectively.



**Figure 3: 2-4 decoder LP and LPI schematics**  
**B. 15-Transistor 2-4 High-Performance Topology**

The low-power topologies presented above have a drawback regarding worst case delay, which comes from the use of complementary  $A$  as the propagate signal in the case of  $D_0$  and  $I_3$ . However,  $D_0$  and  $I_3$  can be efficiently implemented using static CMOS gates, without using complementary signals. Specifically,  $D_0$  can be implemented with a CMOS NOR gate and  $I_3$  with a CMOS NAND gate, adding one transistor to each topology. The new 15T designs present a significant improvement in delay while only slightly increasing power dissipation. They are named “2-4HP” (9 nMOS, 6 pMOS) and “2-4HPI” (6 nMOS, 9 pMOS), where “HP” stands for “high performance” and “I” stands for “inverting.” The 2-4HP and 2-4HPI schematics are shown in Fig. 5(a) and (b), respectively.

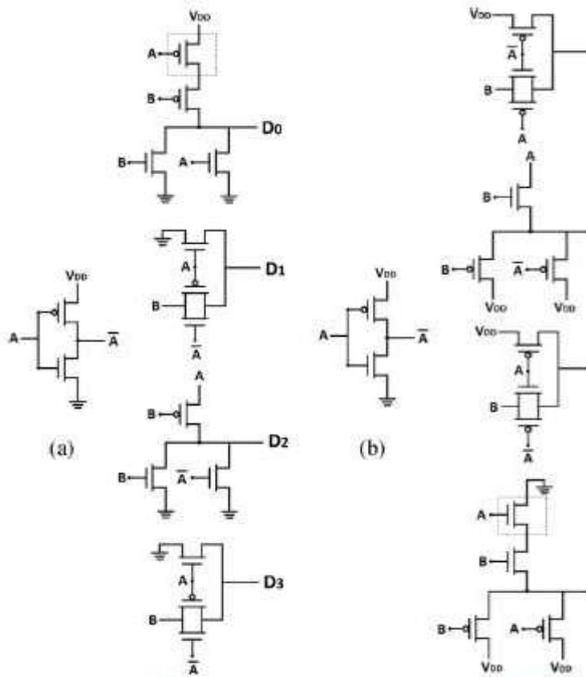


Figure 4: 2-4 decoder High Performance Schematic and HPI schematic

**C. Integration in 4-16 Line Decoders**

PTL can realize logic functions with fewer transistors and smaller logical effort than CMOS. However, cascading PTL circuits may cause degradation in performance due to the lack of driving capability. Therefore, a mixed-topology approach, i.e., alternating PTL and CMOS logic, can potentially deliver optimum results.

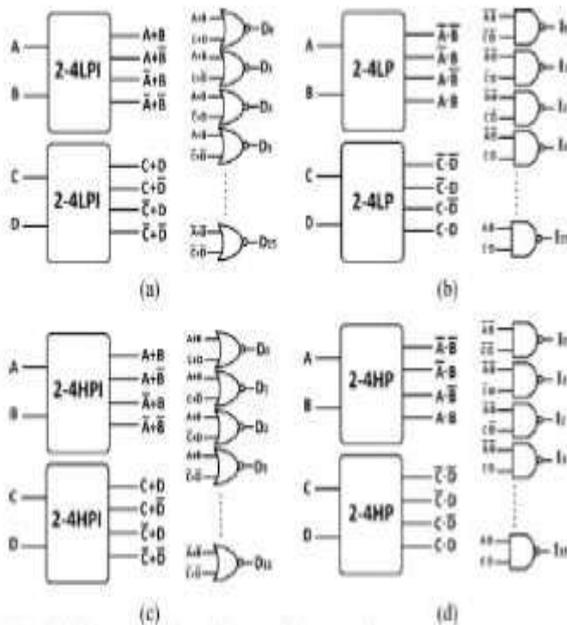


Figure 5: 4-16 Decoder LP, LPI, HP and HPI Schematic

**IV. SIMULATION RESULTS:**

All the implementations are done in Tanner EDA tools and for power calculation we used HSPICE monte Carlo simulation methodology. Below Schematics are from Tanner EDA and

waveforms are from HSPICE tool.

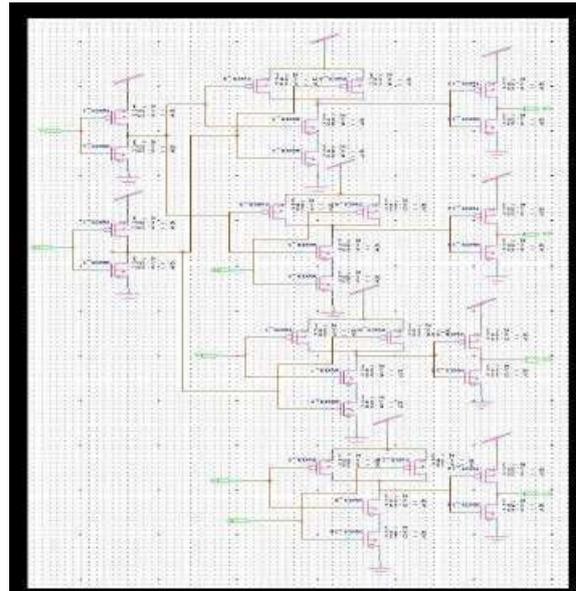


Figure 6: Schematic of CMOS 2-4 decoder

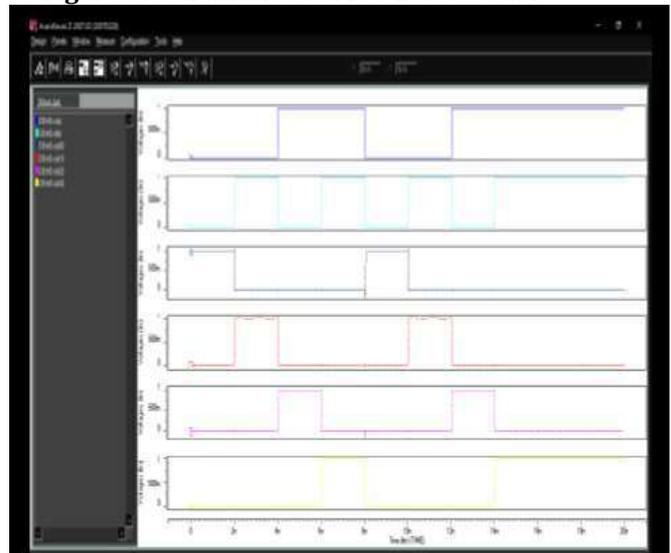


Figure 7: Waveform of CMOS 2-4 Decoder

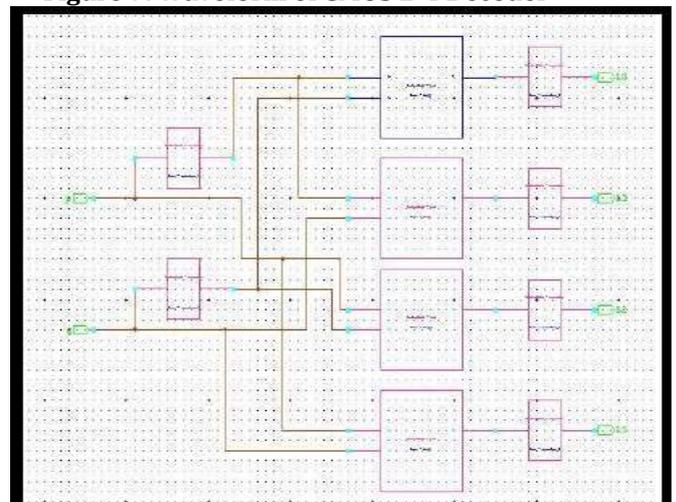


Figure 8: Schematic of 2-4 decoder CMOS Inverter

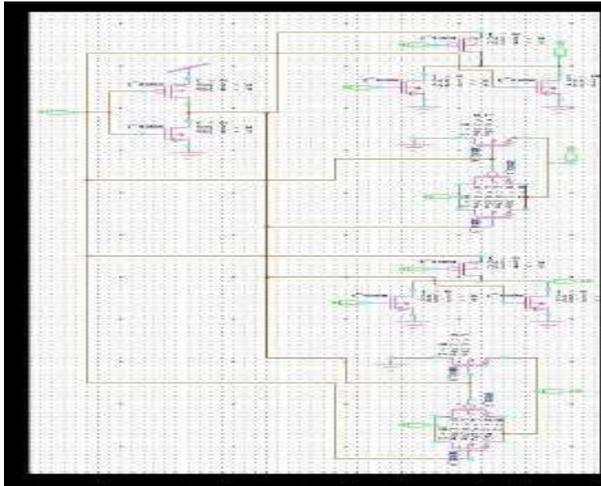


Figure 9: Schematic of Low Power Inverter 2-4 Decoder

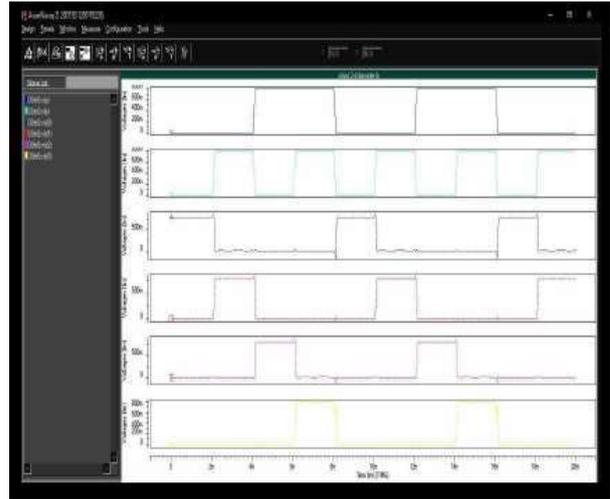


Figure 12: Waveform of High Performance 2-4 decoder

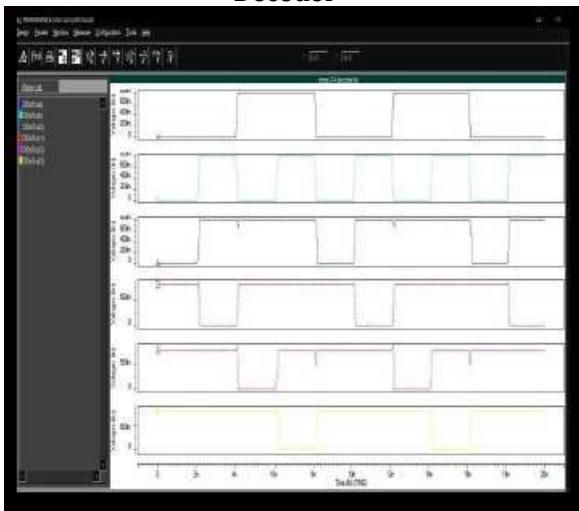


Figure 10: Waveform of Low Power Inverter 2-4 Decoder

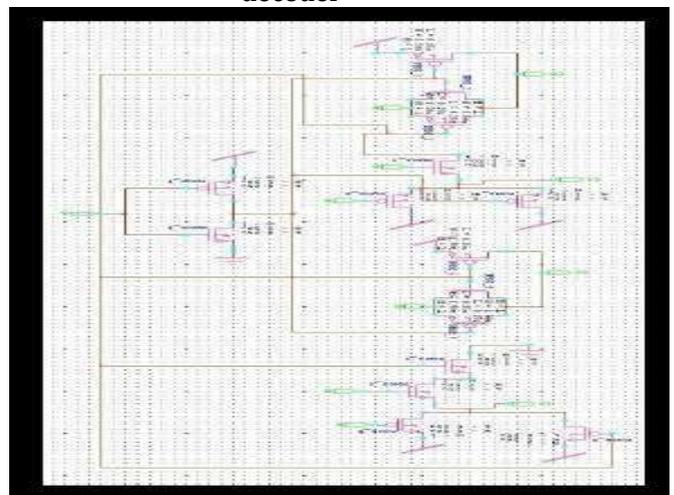


Figure 13: Schematic of High performance Inverter

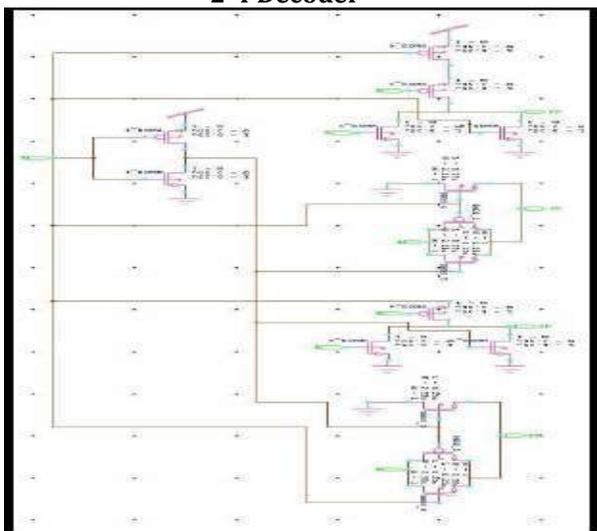


Figure 11: Schematic of High Performance 2-4 Decoder



Figure 14: Waveform of High performance Inverter

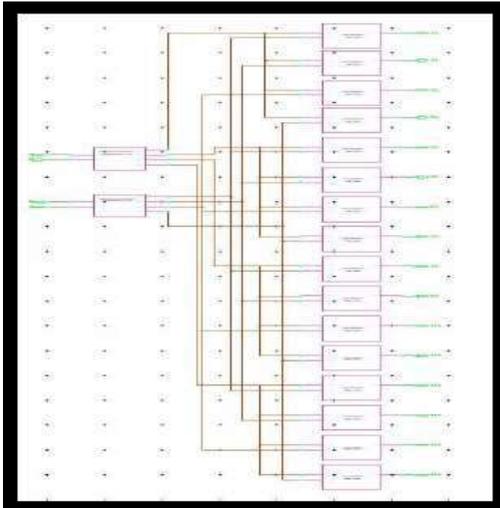
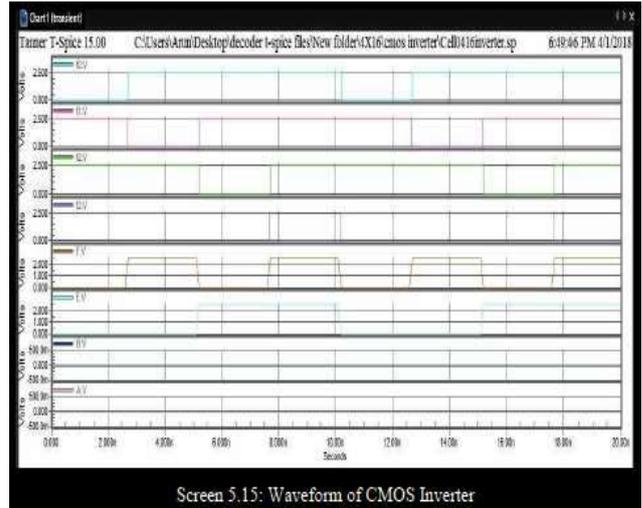


Figure 15: Schematic of CMOS 4-16 Decoder



Screen 5.15: Waveform of CMOS Inverter

Figure 18: Waveform of CMOS Inverter

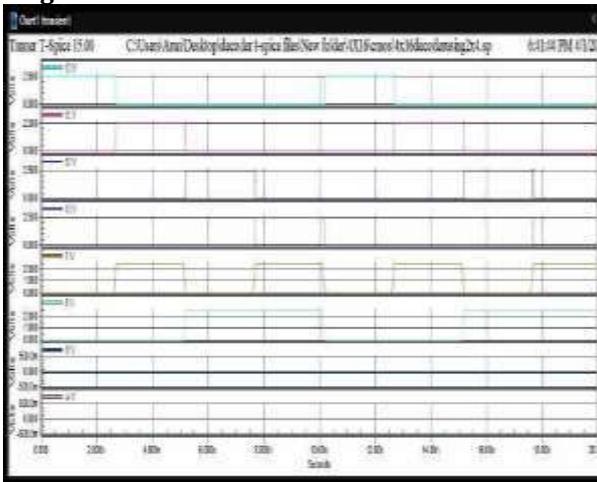


Figure 16: Waveform of CMOS 4-16 Decoder

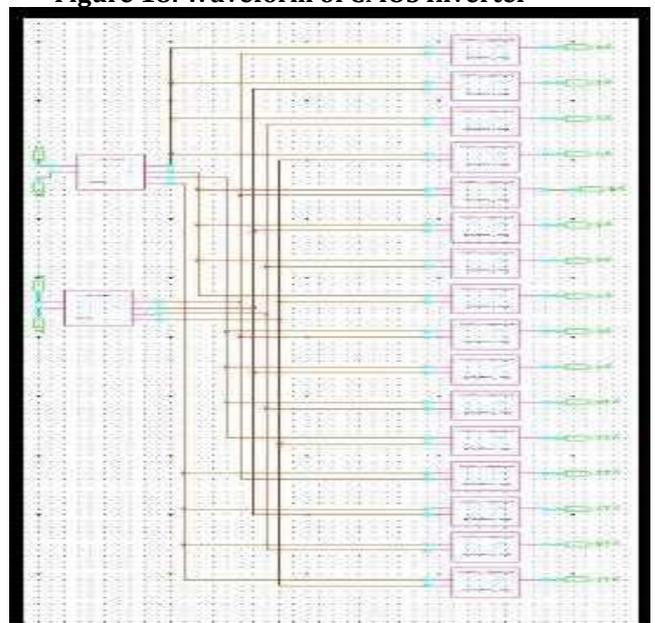


Figure 19: Schematic of LP

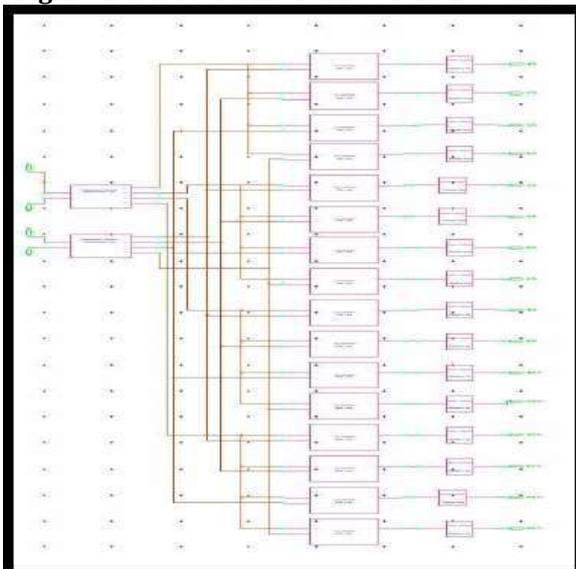


Figure 17: Schematic CMOS Inverter

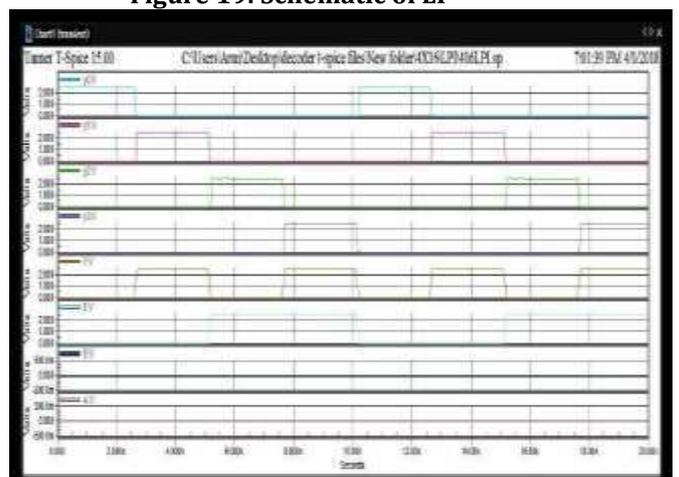


Figure 20: Waveform of LP

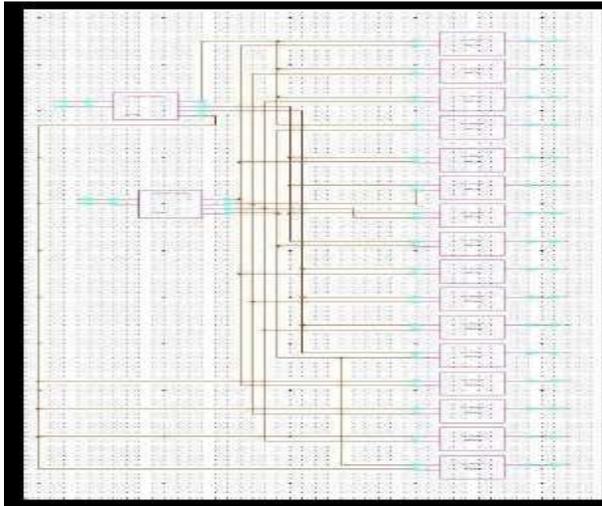


Figure 21: Schematic of LPI

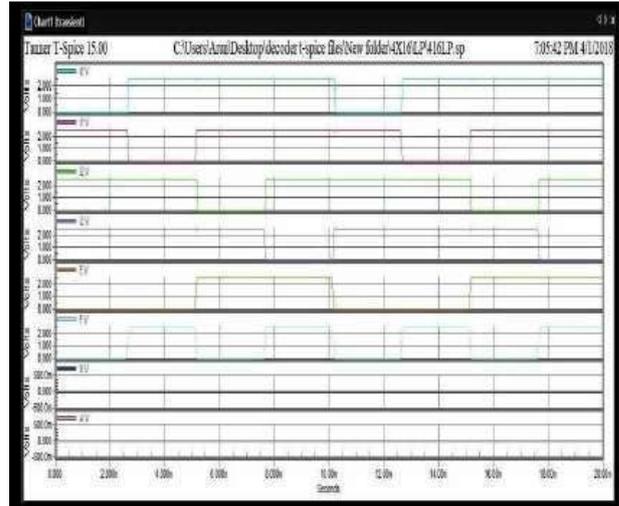


Figure 24: Waveform of HPI

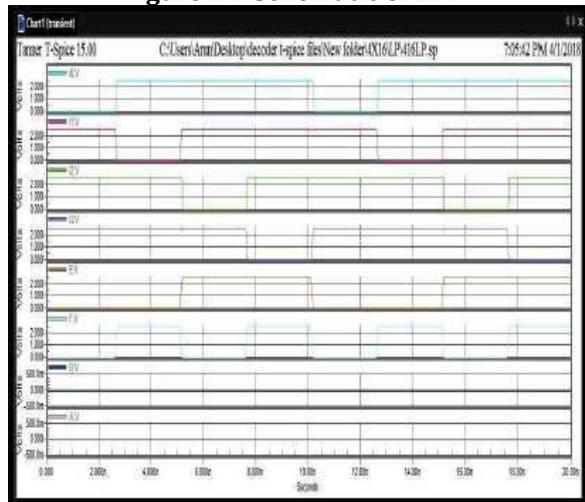


Figure 22: Waveform of LPI

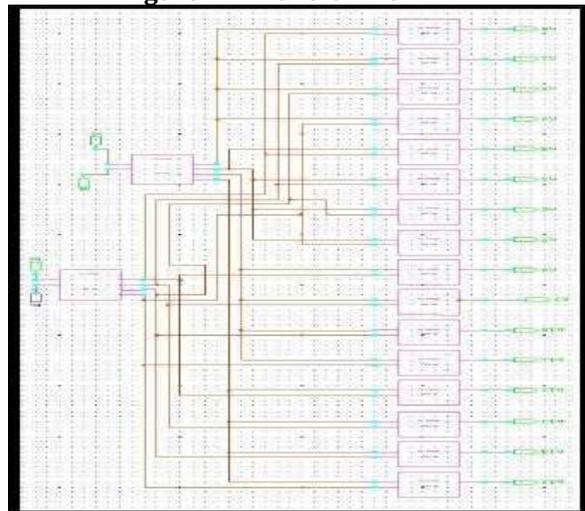


Figure 23: Schematic of HPI

2-4 DEC	0.8 v	1.0 v	1.2 v	4-16 DEC	0.8 v	1.0 v	1.2 v
CMOS	3.73E-07	5.58E-07	8.36E-07	CMOS	1.44E-06	2.32E-06	3.45E-06
LP	1.27E-07	1.47E-07	2.11E-07	LP	9.23E-09	1.28E-06	1.80E-06
HP	1.26E-07	1.46E-07	2.15E-07	HP	1.19E-06	1.68E-06	2.39E-06
CMOS INV	3.17E-07	6.85E-05	1.09E-04	CMOS INV	1.56E-06	2.51E-6	4.12E-09
LPI	1.51E-07	1.99E-07	2.98E-07	LPI			
HPI	2.91E-07	9.41E-07	5.06E-06	HPI	8.10E-07	1.15E-06	1.63E-06

2-4 DEC	0.8 v	1.0 v	1.2 v	4-16 DEC	0.8 v	1.0 v	1.2 v
CMOS	1.89E-09	1.93E-09	1.94E-09	CMOS	1.80E-09	1.89E-09	1.91E-09
LP	1.97E-09	1.97E-09	1.97E-09	LP		1.94E-09	1.95E-09
HP	1.97E-09	1.97E-09	1.97E-09	HP	1.93E-09	1.95E-09	1.95E-09
CMOS INV		5.23E-09	4.81E-04	CMOS INV	4.34E-09	4.16E-09	3.72E-06
LPI	4.06E-09	4.05E-09	4.04E-09	LPI			
HPI	5.489E-09	2.24E-10		HPI	4.21E-09	4.11E-09	4.09E-09

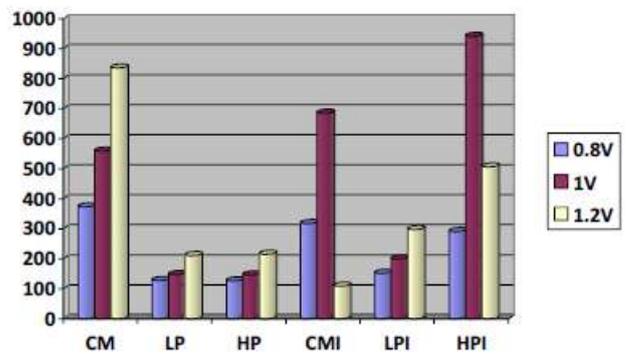
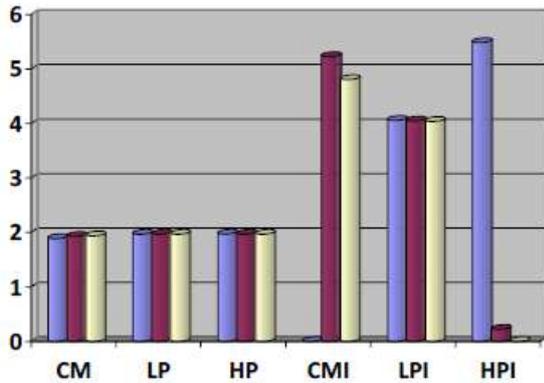


Figure 25: AVERAGE POWER IN NANO WATTS



**Figure 26: PROPAGATION DELAY IN NANO SECONDS**

## V. CONCLUSION

This brief has introduced an efficient mixed-logic design for decoder circuits, combining TGL, DVL and static CMOS. By using this methodology, we developed four new 2–4 line decoder topologies, namely 2–4LP, 2–4LPI, 2–4HP and 2–4HPI, which offer reduced transistor count and improved power delay performance in relation to conventional CMOS decoders. Furthermore, four new 4–16 line decoder topologies were presented, namely 4–16LP, 4–16LPI, 4–16HP and 4–16HPI, realized by using the mixed-logic 2–4 decoders as pre decoding circuits, combined with post decoders implemented in static CMOS to provide driving capability. A variety of comparative spice simulations was performed at 32 nm, verifying, in most cases, a definite advantage in favor of the proposed designs.

A decoder consumes almost 30% of the total power in a memory circuit and hence it becomes mandatory to optimize a decoder circuit in the memory architecture. The main feature of the present work is to optimize the decoder designs in order to achieve better speed and power performance. This work can be extended by using various mixed design styles like DVL, gating technique etc. in this we can obtain better results than CMOS logic where the power consumption and transistor count can be reduced. By this way can obtain less power consumption and high performance operation when compared to CMOS logic design technique.

We can use these decoders in the applications where low power consumption and decoding is necessary such as data multiplexing, 7 segment display and memory address decoding.

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