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ANALYSIS OF DELTA SIGMA MODULATOR OF ORDER 3 AND 4 FOR VARIOUS OPEN SOURCE RESERVATION USING CRFB TOPOLOGY

Dr. T. Ananth Kumar
Assistant Professor, Department of Electronics and Communication Engineering
IFET college of Engineering, Villupuram, Tamil Nadu, India

ABSTRACT

This paper gives a general study for the Sigma Delta Digital to Analog Converter, describes the basic differences between the Nyquist rate DAC & Oversampling DAC. It brings the structure for the order one & two delta sigma modulator. This paper concludes with the SNR vs. oversampling ratio comparison for various order filters. This paper introduces the SNR calculation for various order of Delta Sigma Modulator (DSM) for the loop filter topology chosen as CRFB which is simulated using MATLAB Simulink and Xilinx 14 ISE. The paper concludes with the comparison of all analyzed DSM.

KEYWORDS- *CRFB; DAC; DSM; OSR;*

I. INTRODUCTION

The growth of multimedia systems has been increased with the demand for an audio digital-to-analog converter (DAC), the demand for low-cost, wide dynamic range and high linearity of DAC. Since It is inherently benefited, Delta-sigma modulation (DSM) is the most suitable DAC topology to satisfy these requirements, which reduces the bits of input digital signal at the cost of increasing sample rate and a great many of digital circuits. The area and the intricacy of the analog part can be greatly condensed and the implementation of digital circuit is very convenient by using developed digital signal process and CMOS technique. Therefore the cost of a DAC can be decreased and that's why the topology of DSM is popular now.

In actual application the tradeoff among power, stability and DR must be made. Large DR needs high over sample rate and multi-bit quantizer, which will increase power and the difficulty of the implement of the circuit. For stability multibit quantizer is needed for high order DSM but it will increase the difficulty of the internal design of DAC. So the over sample rate and the number of the bits of the quantizer must be chosen seriously in order to achieve those anticipated goals. [1]

II. DELTA SIGMA DAC ARCHITECTURE

A general block diagram for a sigma-delta D/A converter is depicted in Figure 1. It consists of four functionally different parts. In the first phase, the sampling rate of the input discrete-time signal is increased using an interpolator filter. In the second phase, the noise shaper converts an n-bit input data stream into a 1-bit data stream. This data stream is converted in the third phase into an analog signal using a 1-bit D/A converter. The role of the noise sharper is to keep the noise generated by the quantization as low as possible in the baseband by shaping and moving this noise out of the baseband.

The final phase consists of removing the out-of-band noise using an analog low pass filter.

The major obstacle in the sigma-delta D/A converter design is the efficient small area integration of the interpolator. In this paper, we use similar ideas for designing interpolators for D/A converters. We report a novel high performance linear-phase FIR filter structure which can be easily implemented in a small area. The optimization is performed in such a way that the overall interpolator contains no general multipliers and very few data memory locations. This is achieved by using several interpolation stages with each filter stage containing a small number of delay elements and arithmetic operations.

A. Oversampling and The ΔΣ DAC

The Nyquist sampling theorem states that to reproduce a signal faithfully by means of samples taken at regular intervals it is necessary to sample the signal at a rate that is greater than twice the highest frequency present in the signal. Generally DACs sample at a rate that is a bit higher than the Nyquist rate. Sigma-delta converters, however, are different. Because each digital word output by a sigma-delta converter is the average of many samples, the converter must sample at many times the highest frequency we are interested in seeing. The sigma-delta converter allows us to get very accurate results using very simple analog circuitry. The price we pay is the need to sample the signal very quickly.

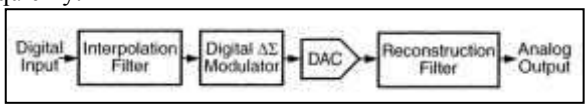

Figure 1: AUDIO DAC Architecture

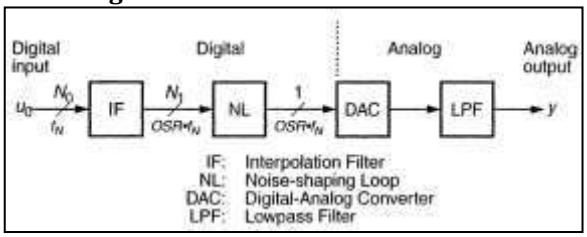

Figure 2: Block Diagram of ΔΣ DAC

The noise-shaping loop NL reduces the word-length of its input signal to a few (1-6) bits. If a single-bit NL output is used, then the linearity requirements for the DAC following the NL can be relaxed. The NL output must contain a faithful reproduction of the input signal $u_0(n)$ in the baseband, but it will also include the filtered truncation noise caused by the reduction of the word-length in the loop. The spectrum of the NL output signal is schematically illustrated in Figure 3.

As well as reducing the cost, oversampling can be used to increase the resolution of DAC. If the converter has a step size of q volts then the error e (which appears as quantization noise) of a quantized sample takes values between -q/2 and +q/2. If we assume that the input signal is equally likely to take any value within one quantization interval, then we can assume that the probability density function for the noise signal is uniform. Therefore the quantization noise power can be calculated as the average squared value of e:

$$Q_N = \frac{1}{q}\int_{-q/2}^{q/2} e^2 de = \frac{1}{3q}\, e^3|_{-q/2}^{q/2} = \frac{q^2}{12} \quad \dots(1)$$

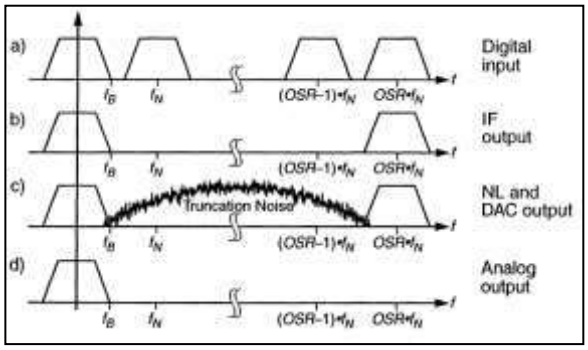

Figure 3: Signal and Noise Spectra in a ΔΣ DAC

B. Delta Sigma Modulator

A sigma-delta modulator is a non-linear system incorporating feedback. Not surprisingly, the modulator may display limit cycle oscillations that result in the presence of periodic (tone) components in the output.

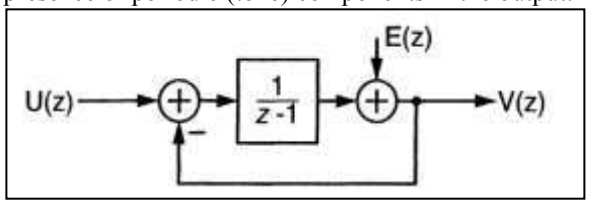

Figure4: Z Domain Model for ΔΣ Modulator

The simplest ΔΣ modulator is a first-order loop containing an integrator.

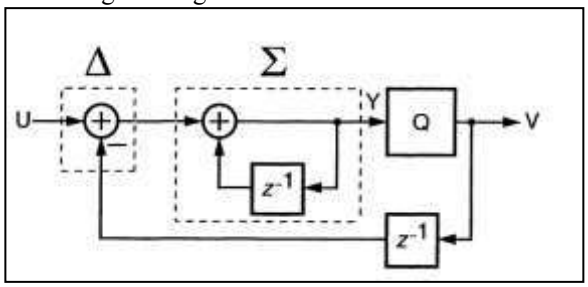

Figure 5: Z Domain Block Diagram of First Order ΔΣ Modulator (MOD1)

From the figure 5,

$$y(n) = y(n-1) + u(n) - v(n-1) \quad \dots(2)$$

And hence combining equations for n=1, 2, 3…N

$$y(N) - y(0) = \sum_{n=0}^{N} [u(n) - v(n-1)] \quad \dots(3)$$

Where v show the outcome of modulator.

Thus, for a dc input u, if we allow the circuit to operate for a sufficiently long time, the average value of the

digital output v will become an arbitrarily good approximation of the input. This average value can be recovered by cascading a digital lowpass filter with the $\Delta\sum$ loop.

The simplest way to construct a second-order modulator from MOD 1 is to replace the quantizer within MOD 1 with another copy of MOD1. The resulting structure is shown in Figure. [3]

$$V(z) = U(z) + (1 - z^{-1})^2 E(z)$$

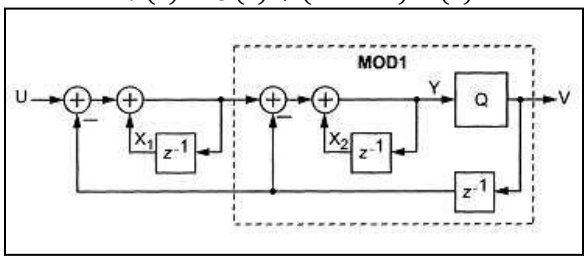

Figure 6: A second-order $\Delta\sum$ modulator (MOD2) obtained by replacing the quantizer in MOD1 with another copy of MOD1

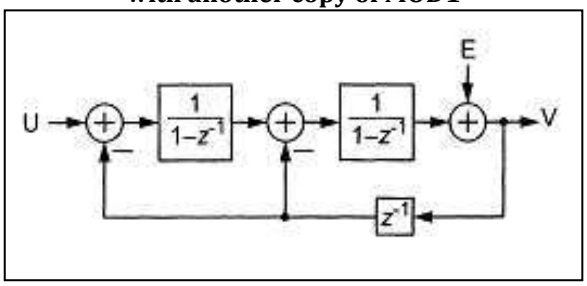

Figure 7: Linear Model second-order $\Delta\sum$ modulator (MOD2)

The Loop filter can be realized in various topologies CIFB (Cascade-of-integrators, feedback form), CIFF (Cascade-of-integrators, feed forward form), CRFB (Cascade-of-resonators, feedback form) & CRFF (Cascade-of-resonators, feed forward form). In the next section the related work is done using the topology CRFB.

The CRFB structure for even & odd order loop filter is given by figure

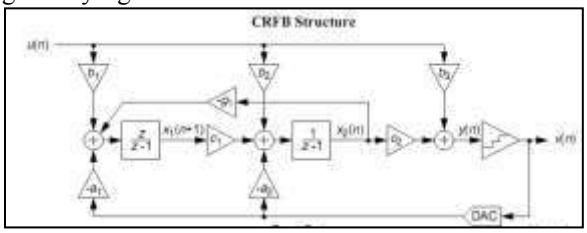

Figure 8a: CRFB Structure for Even Order

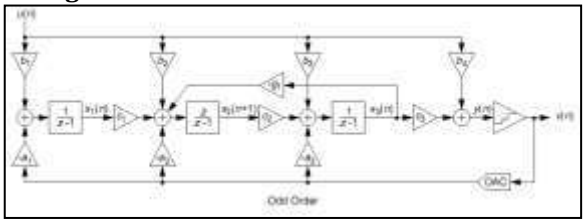

Figure 8b: CRFB Structure for Odd Order

III. RELATED WORK

Specification of Our Work:

- Loop Filter Order: 3rd & 4th
- OSR (Over Sampling Ratio): 16 & 32

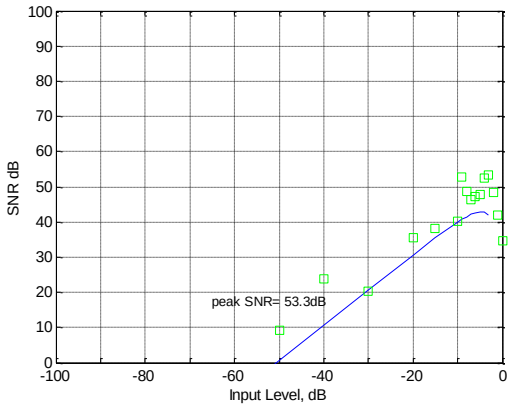

Figure 9a: SNR vs. Input Amplitude for Third Order Sigma Delta Modulator with OSR as 16 using CRFB topology

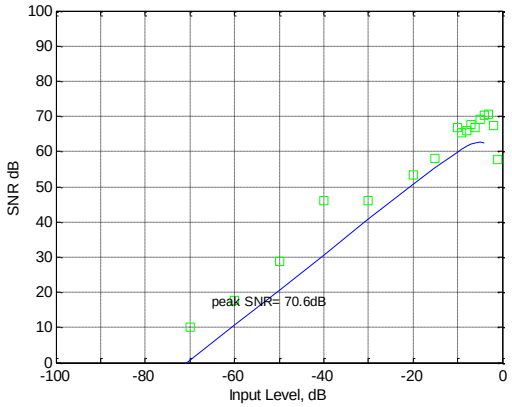

Figure 9b: SNR vs. Input Amplitude for Third Order Sigma Delta Modulator with OSR as 32 using CRFB topology

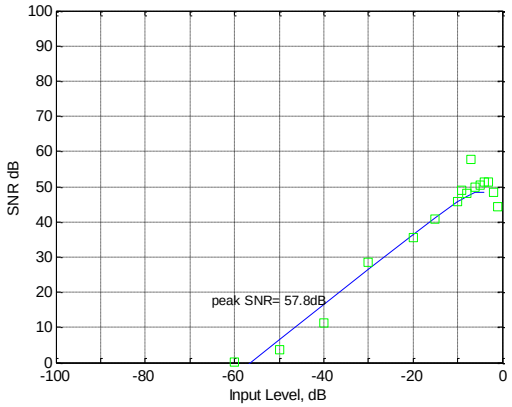

Figure 9c: SNR vs. Input Amplitude for Fourth Order Sigma Delta Modulator with OSR as 16 using CRFB topology

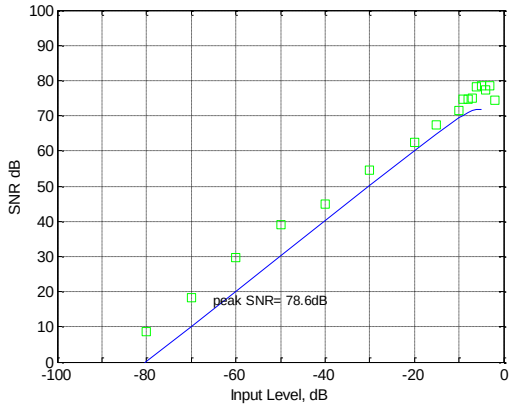

Figure 9d: SNR vs. Input Amplitude for Fourth Order Sigma Delta Modulator with OSR as 32 using CRFB topology

IV. RESULTS

Figure 10 depicts the relationship between quantization noise, OSR, and modulator order by showing the signal to noise ratio (SNR) vs. the OSR for a first, second, and third order modulator. The graph illustrates that as the OSR increases, the noise decreases (SNR increases) and that as the order of the modulator increases, the noise decreases.

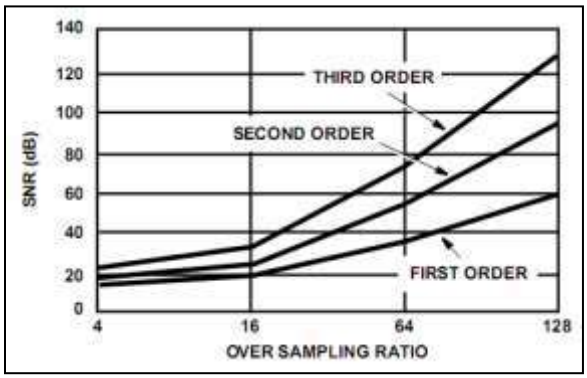

Figure 10: SNR vs. Oversampling Ratio for ΔΣ Modulator

Table 1 shows the comparison among the Delta Sigma Modulator of various orders with different OSR.

Table 1: Comparison of Various DSM

DSM Order	OSR	Max. SNR (in dB)
3	16	53.3
3	32	70.6
4	16	57.8
4	32	78.6

In future, we can implement the HDL code for the above mentioned DSM & compare the same with respect to the hardware requirement (LUT, slices viz.), Maximum frequency of Operation.

V. CONCLUSION

The basic principles of D/A conversion with sigma-delta modulators are reviewed. The techniques of oversampling and noise shaping allow the use of relatively to perform high resolution conversion. Thus, the various order Delta Sigma Modulator design and SNR vs. Oversampling ratio comparison is explained.

VI. REFERENCES

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